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4500 Digital Storage Oscilloscope

Service Manual

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TWX/TELEX # 910-338-0256

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PREFACE

WARNING:

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions in this manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at this own expense will be required to correct the interference.

The following procedures may help to alleviate the radio or television interference problems:

1. Reorient the antenna of the receiver receiving the interference.

2. Relocate the equipment causing the interference with respect to the receiver (move or change relative position).

3. Reconnect the equipment causing the interference into a different outlet so the receiver and the equipment are connected to different branch circuits.

4. Remove the equipment from the power source.

NOTE:

The user may find the following booklet prepared by the FCC helpful: How to Identify and Resolve Radio-TV Interference Problems. This booklet is available from the U.S. Printing Office, Washington, D.C. 20402. Stock No. 004-000-00345-4.

This manual provides specifications, detailed theory of operation, calibration, and alignment procedures for the 4500 Digital Storage Oscilloscope. This manual was written for use by technicians and field service personnel experienced in the alignment and calibration of complex electronic equipment.

The material in this manual is up to date at the time of publication, but is subject to change without notice.

Copies of this publication and other Gould, Inc., Design and Test Systems Division publications may be obtained from the Gould sales office or distributor serving your locality.

RELATED PUBLICATIONS

4500 Digital Storage Oscilloscope Users Manual,
Publication Number 0285-0212-10

For assistance with the product, please call Gould, Inc., Design and Test Systems Division customer service on the toll-free, hot-line numbers listed below:

National (800) 538-9320/9321

California (800) 662-9231

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CHAPTER 1 GENERAL INFORMATION

INTRODUCTION

This manual provides detailed Theory of Operation, Alignment, Calibration, and Maintenance procedures for the Gould Design and Test Systems Division 4500 Digital Storage Oscilloscope.

The manual is organized as follows:

Chapter 1 provides a general introduction to the 4500 Digital Storage Oscilloscope service manual including a general description of the 4500 features and specifications.

Chapter 2 describes the performance verification procedure for the 4500 and includes a list of recommended test equipment.

Chapter 3 explains the operation of self-test, power-up and built-in diagnostics for the 4500.

Chapter 4 contains detailed alignment and calibration procedures.

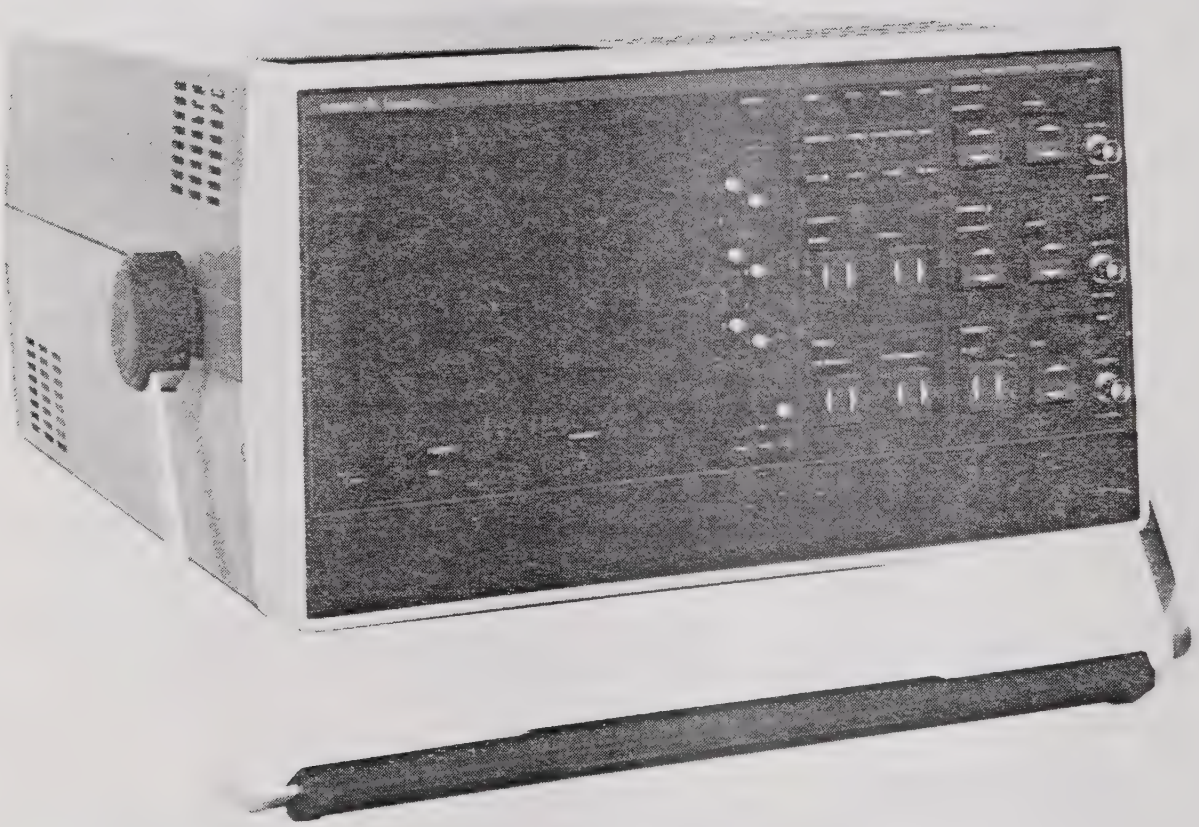
Chapter 5 contains the theory of operation at the block diagram level followed by a detailed theory to the component level with references to the schematics for each board.

Chapter 6 contains the schematic drawings, list of materials, and assembly drawings for each board.

GENERAL DESCRIPTION

The 4500 Digital Storage Oscilloscope, Figure 1-1, is an 8088 microprocessor-based, dual-channel digital storage oscilloscope with 8-bit resolution and a 35-MHz bandwidth. The 4500 provides fast, repeatable waveform recording. Data acquisitions are easily manipulated for accurate measurement.

The 4500 can be used as a stand-alone instrument or as part of a computer controlled system. The GPIB and RS-232 interfaces allow the 4500 to be completely controlled from another computer or 4500. The Interface board contains direct memory access circuits that permit direct external access to data in the fast store memories.



4500-0300

Figure 1-1. 4500 Digital Storage Oscilloscope

FEATURES OF THE 4500

User-Friendly Front Panel - The 4500 is controlled like a conventional oscilloscope using volts and seconds/division terminology. Rocker switches are used to set the most frequently changed parameters. A master menu allows selection of a variety of specific control options, thereby reducing the number of front panel controls.

Easy to Read Displays - The CRT display is vertically-scanned raster type with resolution of 512 by 500. Selections allow display of status parameters only and trace displays with or without menu and graticule.

Auto Setup - When this feature is selected, the 4500 analyzes the input signals and automatically sets the display parameters to produce the best possible trace display.

Data Acquisition - The 4500 samples, digitizes, and stores 1000 discrete points (2000 in single channel mode) on each input channel at sampling rates up to 100 MHz.

Buffer Memories - Two buffer memories can be used as reference memories for acquired signals.

Cursors - Two cursors can be used to make voltage, time, and frequency measurements of a displayed waveform.

Display Interpolators - The 4500 offers sine, linear, and dots display interpolators.

Signal Averaging - For measurement of repetitive waveforms in a noisy environment, the user may select signal averaging to improve the signal to noise ratio by up to 16 dB.

Roll Mode - For waveforms with slow sweep speed, Roll mode shows the acquired waveform rolling across the display much like an oscillographic recorder.

Scroll Mode - Sequential acquisitions are automatically displayed below previous acquisitions when scroll mode is selected.

1 VS 2 Mode - The trace 1 vs 2 mode shows data samples of the two signal traces in X vs Y format.

Setup Store and Recall - Up to five setup states can be stored in non-volatile memory for later recall.

Automatic Calibration - Measurement precision and accuracy are maintained through periodic internal calibration of the analog-to-digital converters.

SPECIFICATIONS

Table 1-1 presents the electrical and environmental specifications for the 4500 Digital Storage Oscilloscope.

Table 1-1. 4500 Specifications

PARAMETER	SPECIFICATION
Channel A and B Inputs	
Input Impedance; all ranges:	1 Mohm ±1% in parallel with 30 pF ±5%.
Input and Offset Voltage Ranges:	

Sensitivity Volts/Div	1 LSB Resolution	Recorded Full Scale Range	Offset Resolution	Offset Voltage Range
1 thru 10 mV	0.31 mV	80 mV	2 mV	±2 V
20 mV	0.62 mV	160 mV	4 mV	±2 V
50 mV	1.56 mV	400 mV	10 mV	±2 V
100 mV	3.23 mV	800 mV	20 mV	±20 V
200 mV	6.25 mV	1.6 V	40 mV	±20 V
500 mV	15.60 mV	4.0 V	100 mV	±20 V
1 V	31.30 mV	8.0 V	200 mV	±64 V
2 V	62.50 mV	16.0 V	400 mV	±64 V
5 V	156.00 mV	40.0 V	1 V	±64 V

Amplifier Bandwidth:	-3 dB at 35 MHz.
ADC Resolution:	8 bits; 1 part in 256.
Input Coupling:	DC, AC (AC -3 dB at 2.5 Hz).
Channel Isolation:	-60 dB at 35 MHz.
Maximum Input Voltage Without Damage: (DC + Peak AC):	±500 V at 1 kHz or less.
Noise:	< 0.2% of full scale RMS.
DC Differential Nonlinearity:	≤ ±0.2% of full scale ±1/2 LSB.
DC Non Linearity:	≤ ±0.4% of offset ±0.2% of offset range.

Table 1-1. 4500 Specifications (Continued)

PARAMETER	SPECIFICATION

Channel A and B Inputs (Continued)

Absolute Offset Voltage Accuracy:
(No offset applied) ±0.5% of offset ±0.2% of offset range.

Absolute Voltage Accuracy:

DC to 1 MHz ±1% of reading
±0.4% of recorded full scale range.

1 MHz to 2 MHz ±2% of reading
±0.8% of recorded full scale range.

2 MHz to 10 MHz ±5% of reading
±1.6% of recorded full scale range.

Overall AC Performance: Complete system AC performance, including ADC. Procedure and equipment lists required to replicate these tests are available from Gould upon request.

Effective resolution of a half scale sinusoid single sweep recording:

Signal Frequency	Effective Bits	Dynamic Range
1 MHz	7.1	42.7 dB
5 MHz	6.6	39.7 dB
10 MHz	6.1	36.7 dB
20 MHz	5.3	31.9 dB
35 MHz	5.1	30.7 dB

Transient Response: Relative error after 3/4 full scale step.

Time After Step	Relative Error
After 20 nsec	0 to -3%
After 40 nsec	±1%

Auto Calibration: Performed every 60 seconds except when the 4500 is armed.

Arm:

Selectable Source: External, Manual, Auto, or Hold.

External Arm Signal: Negative going TTL edge.

Minimum Pulse Width for Certain Detection: 20 nsec at normal TTL levels.

Table 1-1. 4500 Specifications (Continued)

PARAMETER	SPECIFICATION

Trigger

Selectable Source: Channel A, Channel B, External, A auto, B auto, External auto, Line, or Manual.

Coupling: DC/AC(-3 dB at 2.5 Hz).

Filtering: Hi pass -3 dB at 1 kHz;
Low pass - 3 dB at 15 kHz.

Slope/Mode: Selectable either when the source signal passes through a level, or when the source signal leaves or enters a band of ± trigger level, centered around the offset value (band trigger).

Level:

Sensitivity Volts/Division	Trigger Voltage Range	Trigger Resolution
1 mV thru 10mV	±250 mV	2 mV
20 mV	±500 mV	4 mV
50 mV	±1.25 V	10 mV
100 mV	±2.50 V	20 mV
200 mV	±5.00 V	40 mV
500 mV	±12.5 V	100 mV
1 V	±25.0 V	200 mV
2 V	±50.0 V	400 mV
5 V	±64.0 V	1 V

Delay: 0 to 1 screen of pre trigger, 0 to 10 screens of post trigger, or 200 seconds, whichever is less. (Unexpanded displays.)

Trigger Output: TTL level output on rear panel, positive going for trigger, negative going for delayed trigger.

External Trigger: Accepts analog or digital signal. 1 Mohm in parallel with 30 pF input impedance. Level adjustable in range ±5.0 V, in 40 mV steps. Maximum input ±500 V.

Table 1-1. 4500 Specifications (Continued)

PARAMETER	SPECIFICATION
Trigger (Continued)	
Minimum (Internal/External) Pulse Width for Certain Detection:	
20 nsec when overdrive is 10 mV or 5% of trigger voltage range, whichever is greater.	
Maximum Delay from Trigger to First Sample:	70 nsec + one sample period.
Trigger Jitter:	±2 samples intervals worst case; ±1 typical for 0 to 1 screen of delay.
Sweep	
Sample Intervals:	10 nsec to 100 msec/sample internally generated in a 1-2-4 sequence. Continuously variable to 20 nsec/sample with external clock generator.
Sample Interval Accuracy:	100 MHz ±0.01%
Total Sweep Time:	
Single Channel:	2000 x nominal sample interval;
Dual Channel:	1000 x nominal sample interval.
Sweep Speeds:	
Single Channel:	20 nsec/division to 10 sec/division in a 1-2-4 sequence. (20 nsec/division to 1 usec/division are expanded sweep speeds.)
Dual Channel:	20 nsec/division to 10 sec/division in a 1-2-4 sequence. (20 nsec/division to 500 nsec/division are expanded sweep speeds.)
Sweep Expansion:	Controlled by resetting sweep speed and trigger delay after signal acquisition.
Mixed Sweep Speeds:	Sweep speed changes from pre trigger to post trigger sweep speed at the trigger point.
Clock Output:	ECL compatible; 100 MHz.
Clock Gate Input:	ECL compatible; 0 to 20 MHz.
External Clock Input:	ECL compatible; continuous to 50 MHz.
Samples/Sweep:	1000 8-bit samples dual channel; 2000 8-bit samples single channel.

Table 1-1. 4500 Specifications (Continued)

PARAMETER	SPECIFICATION
Display	
Size:	9.5 cm (3.74") high by 12.7 cm (5") wide.
Type:	Vertical raster scan, 500 lines.
Resolution:	500 points horizontally; 512 points vertically.
Graticule:	8 vertical by 10 horizontal divisions internally generated.
Characters:	25 lines each of 62 characters displayable internally or via digital interface. Upper case or lower case special character available.
Intensity:	Adjustable from front panel control.
Number of dots:	(On vertical scan line) 4 maximum; 1 per vertical quadrant.
Linearity:	Better than ±1%.
Analog Plotter Interface (Standard)	
Outputs:	
X or Y:	0 to +10 V Full Scale
Penlift:	TTL output level during valid outputs on X and Y. Polarity selectable.
Speeds:	Selectable X ramp outputs from 1 sec to 100 sec per output trace. Selectable in 1-2-5 sequence.
Interfaces	
Interfaces consist of an IEEE-488 1978 interface, and RS-232C interface, a fast access digital interface, and a fast access analog interface.	
IEEE-488 1978 Interface: This interface facilitates complete Talk/Listen interfacing of the 4500 to a controller, printer, or another 4500. The following specifies the 4500 GPIB capabilities:	
SH1	Source Handshake, complete capability
AH1	Acceptor Handshake, complete capability
T5	Basic Talker, serial poll, talk only mode, unaddress if mla
L4	Basic Listener, unaddress if mta
SR1	Service Request, complete capability
RL1	Remote/Local, complete capability
PP0	Parallel Poll, no capability
DC1	Device Clear, complete capability
DT1	Device Trigger, complete capability
C0	Controller, no capability

Table 1-1. 4500 Specifications (Continued)

PARAMETER	SPECIFICATION
Interfaces (Continued)	
RS-232C Interface:	This interface facilitates complete Send/Receive interfacing of the 4500 to a controller, printer, or another 4500.
Fast Access Digital Interface:	This interface facilitates fast output of stored waveforms. Data rates to 500 k bytes/second. Compatible with Digital Equipment Corporation DR11-B DMA Interface.
Fast Analog Interface:	This interface reconstructs stored digital data with a fast digital to analog converter at rates compatible with analog front ends of signal averagers.
Floppy Disk Accessory	
The floppy disk option is composed of a 5 1/4" single-sided, double-density floppy disk drive housed externally to the 4500. Power and communications to and from the 4500 are via supplied cable.	
Capacity:	40 records of both traces, reference memories and related setup parameters. Data can be transmitted to the floppy or back to the A, B, and reference memories in the 4500.
Probe Accessory	
Tektronic 010-6108-03	
Input Impedance:	10 Mohms in parallel with 13 pF.
Attenuation:	10 X

Table 1-1. 4500 Specifications (Continued)

PARAMETER	SPECIFICATION
Rack Mount Kit	
0112-0293-10 with drawer slides.	
Operating and Storage Conditions:	
Specifications guaranteed from 100 to 300C and less than 5 minutes after auto calibration.	
Operating Temperature:	00 to 500C.
Storage Temperature:	-550 to +850C.
Physical Characteristics	
Height:	21.6 cm (8.5")
Width:	44.5 cm (17.5")
Length:	58.4 cm (23.0")
Mass/Weight:	27.3 kg (60 lbs)
Power	
Input Power:	350 watts maximum.
Frequency:	48 to 66 Hz.
Voltage RMS:	90 to 132 V; 184 to 264 V.
Current RMS:	3.8 A at 92 V.
Fuse:	6 A at 110 V nominal. 3 A at 220 V nominal.
Cable:	2 m (78") long, 3-conductor line cord.

CHAPTER 2 PERFORMANCE VERIFICATION

INTRODUCTION

This chapter provides detailed performance verification procedures for the Gould Design and Test Systems Division 4500 Digital Storage Oscilloscope. Included are recommendations for test equipment.

RECOMMENDED TEST EQUIPMENT

1. The following test equipment is recommended for implementing the performance verification procedure of this manual.

Tektronix model DM 501A digital multimeter or equivalent.

Tektronix model DC 503A universal timer/counter or equivalent, capable of measuring 100-MHz ECL signals with an accuracy of 0.01 percent.

Tektronix model SG 503 levelled sinewave oscillator or equivalent, capable of generating 1.2 V peak-to-peak sinewaves from 625 kHz to 35 MHZ. The sinewaves must not change amplitude as frequency is changed.

Tektronix model FG 502 function generator or equivalent, capable of generating ECL level signals at a frequency of 500 kHz.

Tektronix model TM 504 mainframe (to contain and power the above).

Tektronix model 485 oscilloscope or equivalent, capable of measuring 100-MHz ECL signals.

Wavetek model 142 waveform generator or equivalent, capable of generating 8 V peak-to-peak sinewaves from 2.5 Hz to 50 kHz.

X1 test probe.

Two 50 ohm terminators (BNC female input, BNC male output.)

Three BNC to BNC cables (BNC male connectors on both ends.)

BNC tee coupler. (Two BNC females in and one BNC male out.)

2. For performing calibration of the 4500, the following test equipment is recommended in addition to the above.

Tektronix model PG 506 calibration generator.

Extender board, extension coaxial cable, and input standardizer set.

Part Number	Description
0285-0384-10	Extender Board Set (includes the following six items)
0285-0235-10	Extender for Floppy Disk Controller or Interface board
0285-0235-20	Extender for MPU or CRT Driver board
0285-0240-10	Extender for the Sweep and Record board
0285-0165-10	Extender for either ADC board
0285-0383-10	Extension coaxial cable used when extending an ADC board
0285-0109-10	30 pF Input Standardizer

PERFORMANCE VERIFICATION PROCEDURE

1. The self test procedures that make up the first part of this performance verification procedure exercise most of the 4500 hardware. If all self test procedures pass, a high degree of confidence in 4500 performance may be realized. Other tests are added to verify performance of 4500 functions and specifications not tested by self tests. There are some system functions, such as the external interfaces, that are not tested in this performance verification procedure. This is due to the need for specialized test equipment and software to operate it.

A quick test of system operation can be performed with only a X1 test probe by running the self tests. These are described in steps 2 through 13. Additional information, and photographs of self test results, are shown in Chapter 7 of the 4500 Digital Storage Oscilloscope Users Manual, Publications Number 0285-0212-10.

Note that the 4500 Auto Setup function is used extensively in this procedure. Auto Setup is used to achieve 4500 settings that are required for the tests that specify it.

Instrument Warmup

2. Apply power to the 4500 and allow it to remain on for 20 minutes before performing this procedure.

Initiating Self Test

3. To initiate self test, depress the following front panel keys:

AUTO SETUP
MASTER MENU
TEST, menu key C

The self test menu should appear. Perform each test and verify proper operation as described following.

Sweep and Record Self Test

4. Depress:

SWP/REC, menu key 1

The CRT screen will display a GOOD or BAD indication. All indications should be GOOD.

Trigger Self Test

5. From the SELF TEST menu depress:

TRIGGER, menu key 2

The screen will display a GOOD or BAD indication for channel A and channel B. All indications should be GOOD.

Attenuator Self Test

6. From the SELF TEST MENU depress:

ATTN, menu key 3

Connect:

a X1 probe to the channel A input BNC connector
probe ground to front panel ground test point
probe tip to the front panel CAL test point

Depress:

menu key C

The screen will display a GOOD or BAD indication. The indication should be GOOD.

Perform the same test except with the X1 probe connected to the channel B input BNC connector. The indication should again be GOOD.

Channel A ADC Self Test

7. From the SELF TEST menu depress:

A ADC, menu key 4

The screen will display an expected ramp (sloped line) and an actual ramp. No major difference between the two ramps should be observed.

Channel A DNL Self Test

8. From the SELF TEST menu depress:

A DNL, menu key 5

The display will show a histogram of the differential nonlinearity of the ADC for channel A averaged over a large number of acquisitions.

There are two software versions of this test. In some 4500s (software versions 3.4 and earlier), the DNL test is performed continuously with the results appearing on the display approximately two times a second. In other 4500s (software versions 4.0 and later), the test is performed once each time the A DNL key is depressed. The result takes approximately 12 seconds to appear on the display. In the faster version, less averaging is done and more noise (peak-to-peak variation) is apparent in the result. In the slower version, more averaging is done and the result shows less peak-to-peak variation. The DNL test is designed to ensure a differential nonlinearity of +/- one half LSB.

In the fast version, an acceptable result will show no more than two amplitude peaks greater than +/- 1 division at any one waveform point within five successive tests.

In the slow version an acceptable DNL result will show a histogram on the zero line +/- 1 division. There should be no amplitude peaks greater than +/- 1 division. An example of the slow test is shown in the ADC Calibration Procedure (Figure 4-23).

Channel B ADC Self Test

9. From the SELF TEST menu depress:

B ADC, menu key 6

The screen will display an expected ramp (sloped line) and an actual ramp. No major difference between the two ramps should be observed.

Channel B DNL Self Test

10. From the SELF TEST menu depress:

B DNL, menu key 7

Interpret the results as discussed in step 8 above.

AUTO CAL Self Test

11. From the SELF TEST menu depress:

CAL, menu key 8

All CAL correction factors must be in the range of -128 to +127, or calibration has changed more than AUTO CAL can compensate for. When first calibrated, a 4500 will typically exhibit all its CAL correction factors within the range of 0 to +/- 30.

To terminate the AUTO CAL display depress:

HALT, menu key C

Keyboard Self Test

12. From the SELF TEST menu depress:

KEYBOARD, menu key 9

The display will show 8 columns and 16 rows of zeros, and the key clicker will emit a constant buzz. Depress each front panel key and observe that a single 1 appears on the display in place of one of the zeros. Depress each rocker switch and observe that as the rocker switch is depressed, first a single 1 and then two 1's will appear in place of zeros on the display. Confirm that both a single, and a double 1 may be easily obtained. Test each rocker in both directions (up and down, or left and right).

To terminate the KEYBOARD test:

depress HALT, menu key C

MPU/CRT Self Test

13. From the SELF TEST menu depress:

MPU/CRT, menu key A

The screen will display the software revision; all characters and symbols used in 4500 displays; and all vertical line patterns used to generate graticules, cursors, and the trigger line. The 4500 Digital Storage Oscilloscope Users Manual contains a picture of this display.

Input Impedance

14. Depress:

MASTER MENU
CHNL A, menu key 4
DC, menu key 2, to set the channel A input coupling to DC

Depress:

MASTER MENU
CHNL B, menu key 5
DC, menu key 2, to set the channel B input coupling to DC

Depress:

MASTER MENU
TRIG FLT, menu key 7
DC, menu key 5, to set the trigger input coupling to DC

Set:

CHANNEL A SENSITIVITY to 0.01 V/DIV
CHANNEL B SENSITIVITY to 0.01 V/DIV

Using a DVM measure the input impedance of the channel A, the channel B, and the external trigger front panel inputs. Do this by measuring across the input BNC connectors. Each input should measure 1 Megohm +/- 1%.

Set:

CHANNEL A SENSITIVITY to 0.1 V/DIV
CHANNEL B SENSITIVITY to 0.1 V/DIV

Measure the input impedance of channel A and channel B again. The input impedance should be 1 Megohm +/- 1%.

Set:

CHANNEL A SENSITIVITY to 1 V/DIV
CHANNEL B SENSITIVITY to 1 V/DIV

Measure the input impedance of channel A and channel B again. The input impedance should be 1 Megohm +/- 1%.

Front Panel Test Points

15. Connect:

a X1 probe to the channel A input BNC connector
probe ground to the front panel ground test point
probe tip to the front panel CAL test point

Depress:

MASTER menu key
CAL key located just above the CAL test point
CAL A PROBE, menu key A

The display should show that a X1 type probe has been detected and that the probe error factor is within +/- 0.30%.

Connect:

probe ground to the front panel ground test point
probe tip to the front panel squarewave test point

Depress:

AUTO SETUP key

The display should show the test point squarewave.

Depress:

MASTER MENU key
F(CRSR), menu key 9
V(M), menu key 2 to enable voltage measurement using the major cursor

Depress:

ARM HOLD key to stop acquisition

A stable squarewave should appear on the display. Move the major cursor and note the display readout of voltage at the major cursor position. Verify that at the top of the squarewave the voltage is 3.3 +/- 0.4 V. Verify that at the bottom of the squarewave the voltage is 0 +/- 0.4 V. At the rising and falling edges of the squarewave there should not be any overshoot greater than 0.5 divisions.

Input Noise and Offset, Dual Sweep Speed Switchover

16. Ground both channel inputs using either shorting BNC plugs or 50 ohm terminators.

Depress:

AUTO SETUP key

Set:

CHANNEL A SENSITIVITY to 0.001 V/DIV
CHANNEL A OFFSET to 0 V
CHANNEL B SENSITIVITY to 0.001 V/DIV
CHANNEL B OFFSET to 0 V

Each displayed trace should occupy four or less different voltage levels (i.e., have an amplitude less than or equal to 1 division peak-to-peak). Each trace should be centered within its half of the display screen, plus or minus 1 division.

Set:

PRE TRIGGER SWEEP speed to 100 uS/DIV
POST TRIGGER SWEEP speed to 1 uS/DIV

Depress:

MASTER MENU key
AVG. CAL, menu key 8
16, menu key 3

To speed up acquisition ensure that PART-SUM is off (use menu key 7 to turn partial summing off if it is on).

Set:

TRIGGER DELAY to zero

Note any voltage step in the waveform at the trigger line (the time of transition between the pre trigger and post trigger sweep speeds). The step size must not exceed one and one half divisions (1.5 mV).

17. Repeat step 16, except with a pre trigger sweep speed of 1 uS/DIV, and a post trigger sweep speed of 100 uS/DIV.

Channel A Input Coupling, Trigger Coupling, and Trigger Slope

18. Remove all shorting plugs or 50 ohm terminators from the front panel BNC connectors.

Depress:

AUTO SETUP key
MASTER MENU key
TRIG SRC, menu key 6
A, menu key 1, to select channel A as the trigger source

Set:

CHANNEL A SENSITIVITY to 1V/DIV
POST TRIGGER SWEEP speed to 100 mS/DIV
TRIGGER LEVEL to 0 V

Apply a 2.5-Hz sinewave (a sinewave with a 4 division period) to the channel A input. Using the amplitude control on the sinewave generator adjust the input amplitude for 6 divisions peak-to-peak on the display.

Depress:

MASTER MENU key
CHNL A, menu key 4

Change between AC and DC coupling using menu keys 1 and 2. Verify that the amplitude of the displayed sinewave changes to 4.2 +/- 0.5 divisions peak to peak when AC coupling is active, and back to 6 divisions peak-to-peak when DC coupling is active. Leave the coupling set on DC.

Depress:

MASTER MENU key
TRIG FLT, menu key 7

Change the trigger input coupling between DC and AC using menu keys 5 and 1. Verify that the waveform shifts on the display one half division to the right when coupling is changed from DC to AC, and that the display shifts one half division to the left when the coupling is changed from AC to DC.

Channel B Input Coupling, Trigger Coupling, and Trigger Slope

19. Set:

CHANNEL B SENSITIVITY to 1 V/DIV
POST TRIGGER SWEEP speed to 100 mS/DIV
PRE TRIGGER SWEEP off

Depress:

MASTER MENU key
TRIG SRC, menu key 6
B, using menu key 2

Apply a 2.5-Hz sinewave (a sinewave with a 4 division period) to the channel B input. Using the amplitude control on the sinewave generator adjust the input amplitude for 6 divisions peak-to-peak on the display.

Depress:

MASTER MENU
CHNL B, using menu key 5

Change between AC and DC coupling using menu keys 1 and 2. Verify that the amplitude of the displayed sinewave changes to 4.2 +/- 0.5 divisions peak-to-peak when AC coupling is active, and back to 6 divisions peak-to-peak when DC coupling is active. Leave the coupling set on DC.

Depress:

MASTER MENU key
TRIG FLT, menu key 7

Change the trigger input coupling between DC and AC using menu keys 5 and 1. Verify that the waveform shifts on the display one half division to the right when coupling is changed from DC to AC, and that the display shifts one half division to the left when the coupling is changed from AC to DC.

External Trigger Coupling and Trigger Slope

20. Leave the 4500 set up as it was at the end of step 19. Leave the 2.5-Hz sinewave connected to the channel B BNC connector, but simultaneously connect this sinewave to the external trigger input.

Depress:

MASTER MENU
TRIG SRC, menu key 6

Set:

TRIGGER LEVEL to 0 V

Depress:

MASTER MENU
TRIG FLT, menu key 7

Change the trigger input coupling between DC to AC using menu keys 5 and 1. Verify that the waveform shifts on the display one half division to the right when coupling is changed from DC to AC, and that the display shifts one half division to the left when the coupling is changed from AC to DC.

Change the trigger slope between POS and NEG, using menu keys 7 and 8. Verify that the slope of the waveform at the trigger line is positive when POS is selected, and negative when NEG is selected.

Trigger Filtering

21. Connect:

a 1-kHz sinewave to the channel B input

Set:

CHANNEL A SENSITIVITY to 1V/DIV
CHANNEL B SENSITIVITY to 1V/DIV
POST TRIGGER SWEEP speed to 400 uS/DIV
PRE TRIGGER SWEEP speed to off
TRIGGER LEVEL to 0 V

Depress:

MASTER MENU
TRIG SRC, menu key 6
B, menu key 2

Using the amplitude control on the sinewave generator adjust the input amplitude for 6 divisions peak-to-peak on the display.

Depress:

MASTER MENU
TRIG FLT, menu key 7

Change the trigger coupling from DC, to AC HIPAS using menu key 2, and back to DC using menu key 5. The waveform should shift one half division to the right when AC HIPAS is selected, and one half division to the left when DC is selected.

Set:

the sinewave frequency to 15 kHz
the POST TRIGGER SWEEP speed to 20 uS/DIV

Adjust the sinewave amplitude so the displayed waveform is 6 divisions peak-to-peak. Change the trigger coupling from DC, to AC LOPAS using menu key 3, and back to DC using menu key 5. The waveform should shift one half division to the right when AC LOPAS is selected, and one half division to the left when DC is selected. Change the trigger coupling from DC, to DC LOPAS using menu key 4, and back to DC using menu key 5. The waveform should shift one half division to the right when DC LOPAS is selected, and one half division to the left when DC is selected. Repeat this step except connect the sinewave to the channel A input and select trigger source A.

Line Triggering

22. Leave the unit set up as it was at the end of step 21.

Depress:

MASTER MENU
TRIG SRC, menu key 6
LINE, menu key 7

Verify that the 4500 is triggering by noting a continuous acquisition and display of the 15-kHz sinewave. The line trigger will not be synchronous with the 15-kHz sinewave and the waveform should change its position on the display at the end of each acquisition.

Manual Triggering

23. Leave the unit set up as it was at the end of step 22.

Depress:

MASTER MENU
TRIG SRC, menu key 6
MANUAL, menu key 8

The 4500 should stop triggering and no new acquisitions nor display update should occur.

Depress:

MANUAL trigger key located above the external trigger input connector

A single acquisition and a new display of the 15-kHz sinewave should occur.

Input Bandwidth

24. Set:

CHANNEL A SENSITIVITY to 0.2 V/div
CHANNEL A OFFSET to 0 V
CHANNEL B SENSITIVITY to 0.2 V/DIV
CHANNEL B OFFSET to 0 V
POST TRIGGER SWEEP speed to 400 nS/div
PRE TRIGGER SWEEP speed to off
TRIGGER LEVEL to 0 volts

Depress:

MASTER MENU;
TRIG SRC, menu key 6
A/AUTO, menu key 4

Connect to channel A input:

a sinewave of approximately 625 kHz (1.6 uS period).

Adjust the sinewave's amplitude to 6 divisions peak-to-peak as shown on the 4500 display for channel A. Change the sinewave frequency to 35 MHz. Ensure that the sinewave generator does not change the amplitude of its output when its frequency is changed.

The 4500 display for channel A should now show a waveform that is many cycles of sinewave. The amplitude of the sinewave should be 4.3 to 5.7 divisions peak-to-peak.

Depress:

MASTER MENU;
TRIG SRC, menu key 6
B/AUTO, menu key 5

Connect to channel B input:

a sinewave of approximately 625 kHz (1.6 uS period).

Adjust the sinewave's amplitude to 6 divisions peak-to-peak as shown on the 4500 display. Change the sinewave frequency to 35 MHz. Ensure that the sinewave generator used does not change the amplitude of its output when its frequency is changed.

The 4500 display for channel B should now show a sinewave of 4.3 to 5.7 divisions peak-to-peak.

Channel Isolation

25. Set:

CHANNEL A SENSITIVITY to 1 V/DIV
CHANNEL B SENSITIVITY to 0.001 V/DIV
CHANNEL B OFFSET to 0
POST TRIGGER SWEEP speed to 40 nS/DIV

Input a 35-MHz sinewave to channel A and adjust the sinewave input amplitude for 5 V peak-to-peak. Ground the channel B input with a BNC shorting connector or a 50 ohm terminator. Verify that any signal appearing on the channel B display is less than 5 divisions peak-to-peak.

Set:

CHANNEL B SENSITIVITY to 1 V/DIV
CHANNEL A SENSITIVITY to 0.001 V/DIV
CHANNEL B OFFSET to 0
POST TRIGGER SWEEP speed to 40 nS/DIV

Input a 35-MHz sinewave to channel B and adjust the sinewave input amplitude for 5 V peak-to-peak. Ground the channel A input with a BNC shorting connector or a 50 ohm terminator. Verify that any signal appearing on the channel A display is less than 5 divisions peak-to-peak.

Without changing the input amplitude of the 35-MHz sinewave connect this signal to the external trigger input.

Depress:

MASTER MENU
TRIG SRC, menu key 6
EXT, menu key 3

Set:

CHANNEL A SENSITIVITY to 0.001 V/DIV
CHANNEL A OFFSET to 0 V
CHANNEL B SENSITIVITY to 0.001 V/DIV
CHANNEL B OFFSET to 0 V

Short both the channel A and channel B inputs with shorting plugs or 50 ohm terminators. Any signal appearing on the channel A or channel B display should be less than 5 divisions peak-to-peak.

Plotter Outputs

26. Apply a squarewave to the the channel A input and depress AUTO SETUP.

Set an oscilloscope to X-Y mode and connect the rear panel PLOT X and PLOT Y outputs to the X and Y inputs of the oscilloscope. Set the X any Y sensitivities of the oscilloscope to 5 V/DIV. Using the position controls on the oscilloscope set its zero volt reference point to the center of its display screen.

Depress:

MASTER MENU
PLOTTER, menu key A
MAX, MAX, menu key 2

The oscilloscope display should show a dot at the X=10 V, Y=10 V point.

Depress:

SPEED 1, menu key 5
PLOT, menu key 1

Acquisitions should temporarily halt and the oscilloscope should draw the same waveform that is on the 4500 display.

Select different plotter speeds using menu keys 5 through B. After each speed change press PLOT, menu key 1. The oscilloscope should draw the same waveform as on the 4500 display, but with increasing speed as the menu selected speed number is increased.

Depress MASTER MENU to leave the plotter mode.

Trigger Output

27. Attach a cable from the 4500 channel A input to the rear panel TRIGGER OUT connector.

Depress:

MASTER MENU
TRIG SRC, menu key 6
A/AUTO, menu key 4
AUTO ARM key
AUTO SETUP key

The 4500 display should show a waveform that is low before the trigger line and high after the trigger line. Depress the TRIGGER DELAY rocker switch and verify that the rising edge of the waveform follows the trigger line on the display.

Clock Output

28. With an oscilloscope set to have a 50 ohm input impedance verify that the signal on the rear panel CLOCK OUT connector is a 100-MHz ECL signal. Measure the frequency of this signal with a frequency counter. The frequency should be 100 +/-0.01 MHz.

Clock Gate Input

29. Apply an 8 volt peak-to-peak, 50-kHz sinewave to both channels of the 4500.

Depress:

AUTO SETUP

Set:

CHANNEL A SENSITIVITY to 1 V/DIV
CHANNEL B SENSITIVITY to 1 V/DIV
POST TRIGGER SWEEP speed to 1 uS/DIV

Apply a 500-kHz, ECL level squarewave to the rear panel CLOCK GATE connector. Verify that the waveforms displayed are portions of sinewaves with steps in them at each division. Ensure that there are no overshoot or undershoot spikes at the tops and bottoms of each step.

While observing the display, slowly vary the frequency of the 500-kHz signal throughout the range of approximately 250 kHz to 1 MHz. There should be no overshoot or undershoot spikes at the top or bottom of each step. Note that the steps change shape as the frequency is changed.

Display Intensity Control

30. Rotate the front panel INTENSITY control clockwise. Ensure that the display intensity goes from barely visible to full brightness.

CMOS Memory Data Retention Test

31. Write down the sensitivity and offset voltage of channel A and channel B. Write down the pre trigger and post trigger sweep speed. Enter a nonzero trigger delay and write down this setting. Turn off and then power up the 4500 several times, and then recheck the settings of the above parameters. Ensure CMOS memory has retained its data by noting that these parameters are the same as they were before power was turned off.

Floppy Disk Drive

32. The floppy disk drive is an option. If it is not present, skip this step. Connect any convenient waveform to the channel A and channel B inputs.

Depress:

AUTO SETUP

The waveform should now be displayed. Place a diskette in the disk drive. Be sure that the diskette does not have a write protect tab on it.

Format the disk by depressing:

MASTER MENU
I/O, menu key B
DISK, menu key B
FORMAT, menu key 1
CONFIRM, menu key C

The disk drive light should illuminate. When the light goes off, formatting is complete. If an error message appears, try another diskette to determine if the fault is with the disk or with the drive.

Select and write to file 40 by depressing:

FILE, menu key 2
4, menu key 4
0, menu key A
ENTER, menu key C
WRITE, menu key 4
CONFIRM, menu key C

The disk drive light should illuminate to indicate that the write operation to FILE 40 is occurring. When the light turns off the write operation is complete.

Select and write to file 1 by depressing:

FILE, menu key 2
1, menu key 1
ENTER, menu key C
WRITE, menu key 4
CONFIRM, menu key C

The disk drive light should illuminate to indicate that the write operation to FILE 1 is occurring. When the light turns off the write operation is complete.

Change the input signal to a different waveform so the next recording appears different from the recordings stored on disk.

Depress: AUTO SETUP

Observe the recording of the present input signal.

Select and read file 40 by depressing:

FILE, menu key 2
4, menu key 4
0, menu key A
ENTER, menu key C
READ, menu key 5
CONFIRM, menu key C

After the disk is read the display should show the initial waveform that was stored on disk.

Depress: SINGLE ARM

The display should show the current input signal.

Select and read file 1 by depressing:

FILE, menu key 2
1, menu key 1
ENTER, menu key C
READ, menu key 5
CONFIRM, menu key C

After the disk is read the display should show the initial waveform that was stored on disk.

Depress: Auto File, menu key 3
AUTO ARM

The 4500 should automatically take recordings and store them on disk in each of the 40 files. The file number can be observed incrementing on the menu display. The 4500 will stop recording after file 40.

Disconnect the input signal from the channel A and channel B inputs.

Depress: AUTO SETUP

The display should now show only random noise is being recorded.

Select and read file 25 by depressing:

FILE, menu key 2
2, menu key 2
5, menu key 5
ENTER, menu key C
READ, menu key 5
CONFIRM, menu key C

After file 25 is read the display should show the signal that was recorded prior to its being disconnected from the inputs.

Interface Option Tests

33. Procedures for testing the GPIB, RS-232, and DMA interface circuits are not included here. These interfaces may be tested by connecting and operating the external interface devices as described in the 4500 Digital Storage Oscilloscope User's manual.

CHAPTER 3 DIAGNOSTICS

INTRODUCTION

This chapter provides detailed diagnostic procedures for the Gould Design and Test Systems Division 4500 Digital Storage Oscilloscope.

The 4500 uses Self-diagnostics to verify proper system operation without the need for specialized test equipment. Three types of diagnostics are described in this manual:

(1) Self-Test Diagnostics,
(2) Power Up Diagnostics, and
(3) Built-In Diagnostics.

The Self-Test Diagnostics are accessible by the user and are mostly self-explanatory. These diagnostics are explained in Chapter 2, Performance Verification Procedure and also in Chapter 7 of the 4500 Digital Storage Oscilloscope User's Manual. The Power-Up Diagnostics and the Built-In Diagnostics are described in following paragraphs.

POWER UP DIAGNOSTICS

Each time the system is turned on, it will run some basic power-up diagnostics. These diagnostics will also start again when the RESET switch on the MPU board is pressed. These diagnostics will only operate when the test selection switches on the MPU board are set for a normal operating mode. Refer to the 4500 Built-in Diagnostics section for switch selection descriptions.

Four LED's on the MPU board indicate status of the power-up diagnostics. Each LED extinguishes when that diagnostic test passes. If a failure occurs, the system will lock up and that test's LED will remain lit.

LED #1 - Tests basic CPU functions including interrupt checks and initiation of the other power-up diagnostics.

LED #2 - Tests the EPROM checksums of the system software located on the CRT Driver board.

LED #3 - Tests the MPU RAM's for Read/Write errors.

LED #4 - The system is checked to see if the interface or floppy disk option is present. Auto Cal is also initialized, and if the system does not complete the recording process this test will fail.

4500 BUILT-IN DIAGNOSTICS

1. The following diagnostics reside in ROM and are an integral part of the 4500. A diagnostic is selected by setting the 8 position DIP switch on the top of the MPU circuit board. The diagnostic is initiated by depressing the reset switch next to the DIP switch or turning power on if the 4500 is off. The necessary DIP switch settings to select the various diagnostics are given as two hexadecimal digits. These digits represent eight bits, which in turn represent the settings of the eight switches. The MSB represents switch 8 and the LSB represents switch 1. A binary 0 represents a closed switch and a binary 1 an open switch. For example, in the case of diagnostic 07H (H specifies hexadecimal) represents switches 1 to 3 open and switches 4 to 8 closed.

2. Switch settings 0 through 12H select diagnostics. Setting 7FH selects normal 4500 operation, except with AUTO CAL disabled. Disabling AUTO CAL is necessary when aligning the ADC. Setting FFH selects normal 4500 operation with AUTO CAL enabled. The 4500 should be returned to the FFH setting after all testing operations are completed.

3. All diagnostics begin by clearing the CRT and then displaying a message "DIAG nn", which shows the test being executed where nn represents the hexadecimal number of the diagnostic selected. Tests 03H (FILL SCREEN), 06H (RAM TEST), and 07H (WRITE 16K) quickly write over this message as the memory containing this message is tested.

4. Following is a quick reference to the available diagnostics. A more complete description of each is provided following this list:

00H	Interrupt system test
01H	Write any byte to any I/O address
02H	Read and display byte from any I/O address
03H	Fill screen with byte from DIP switch
04H	Trace generator test
05H	Graticule generator test
06H	Dynamic RAM and CMOS RAM test
07H	Write to dynamic RAM (0 - 3FFFH)
08H	Read from dynamic RAM (0 - 3FFFH)
09H	Write to CMOS RAM (4000H - 40FFH)
0AH	Read from CMOS RAM (4000H - 40FFH)
0BH	Rotating LED pattern
0CH	Trigger level adjustment aid
0DH	Cal DAC adjustment aid
0EH	CRT alignment test pattern
0FH	CMOS RAM power down data retention test
10H	Channel A alignment aid
11H	Channel B alignment aid
12H	ROM checksum test

5. Diagnostic 00H -- Interrupt system test

Provides the following display:

```
TIMER - - -     0
FRONT-END -     0
SPURIOUS  -     0 LEVEL =
```

Enables interrupts, counts the number of interrupts of each kind that occur, and displays these numbers. If interrupts are operating properly, the timer interrupt should occur 50 times per second and no front-end or spurious interrupts should occur.

6. Diagnostic 01H -- Write any byte to any I/O address

Begins by writing 01H to port 01H. The value written is incremented indefinitely and written again to the same port at a frequency of approximately 200 KHz. If the DIP switch is changed, the new value selects another I/O port address. This port is then written to, and the port address is displayed.

7. Diagnostic 02H -- Read and display byte from any I/O address

Begins by reading from port 02H and displaying the data read. If the DIP switch is changed, the new setting selects another I/O port address. This port number is shown on the display and this port is read from. The value read is displayed.

8. Diagnostic 03H -- Fill screen with byte from DIP switch

Fills the display with a character selected by the DIP switch. When first invoked, the character corresponding to 03H is displayed throughout the CRT screen. Changing the DIP switch causes a new character corresponding to the new DIP switch value to appear throughout the CRT screen.

9. Diagnostic 04H -- Trace generator test

Displays 4 traces on the CRT. All possible traces values are attempted in an incrementing sequence. Display should appear to be 4 horizontal lines rolling upwards with some momentary vertical line flashes.

10. Diagnostic 05H -- Graticule generator test

When a graticule is drawn during 4500 operation, the display circuitry selects the desired vertical line pattern to draw at each scanline from the graticule ROM. The graticule generator test diagnostic reads each available pattern from the graticule ROM and repeats the pattern on 8 adjacent scanlines, starting from the left side of the display screen.

11. Diagnostic 06H -- Dynamic RAM and CMOS RAM test

Performs a check of dynamic RAM and CMOS RAM. Dynamic RAM resides at addresses 0000H through 3FFFH. CMOS RAM resides at addresses 4000H through 40FFH. The test fills the RAMS with incrementing values while incrementing addresses. The test reads the values back and checks the value while decrementing addresses. The value written into the first address is then incremented and the test repeated. If this procedure is performed for an extended period, the test writes and checks every possible value at every address. However, most failures appear in a short time. When an error occurs, the following message is displayed:

ERROR: ADDR xxxx WROTE: xx READ: xx

The address, the data value which should have been read, and the data value actually read, are shown. The processor then enters a loop which writes the value that failed to the address that failed and reads back data from this address. This loop repeats indefinitely.

12. Diagnostic 07H -- Write to dynamic RAM

Writes 55H to the dynamic RAM memory at addresses 0000H through 3FFFH. Memory locations are incremented and writing continues indefinitely.

13. Diagnostic 08H -- Read from dynamic RAM

Reads from the dynamic RAM memory at addresses 0000H through 3FFFH. Memory locations are incremented and reading continues indefinitely. No messages other than the diagnostic number are displayed on the CRT.

14. Diagnostic 09H -- Write to CMOS RAM

Writes 55H to the CMOS RAM memory at addresses 4000H to 40FFH. Memory locations are incremented and writing continues indefinitely.

15. Diagnostic 0AH -- Read from CMOS RAM

Reads from the CMOS RAM memory at addresses 4000H through 40FFH. Memory locations are incremented and reading continues indefinitely. No messages other than the diagnostic number are displayed on the CRT.

16. Diagnostic 0BH -- Rotating LED pattern

Illuminates LED 1, LED 2, LED 3, and LED 4 individually in sequence with a short pause between each LED.

17. Diagnostic 0CH -- Trigger level adjustment aid

Sets both analog trigger DACs to negative full scale by outputting the value FFH to port 30H and port 40H, or to positive full scale by outputting the value 00H to port 30H and port 40H. Each time the MASTER menu key is depressed, the output value is changed and retransmitted. The current value is displayed on the CRT.

18. Diagnostic 0DH -- CAL DAC adjustment aid

Writes two different values to the DAC on each ADC board that generates the voltage used during AUTO CAL. The DAC on each ADC board also generates the offset voltage when AUTO CAL is not operating. During this diagnostic, the number 01 or 02 appears on the display. When 01 is displayed, the DAC is set to output +10 V. When 02 is displayed, the DAC is set to output -10 V. These settings are used to adjust the DAC circuitry so the +10 V and -10 V values are within tolerance. The setting may be changed from +10 V to -10 V or from -10 V to +10 V by depressing the MASTER MENU key on the front panel. The voltage is measured on the ADC board at test point TP2.

19. Diagnostic 0EH -- CRT alignment test pattern

Seventeen equally spaced vertical lines and thirteen equally spaced horizontal lines are generated on the CRT. This test may be used as an alignment pattern for adjusting the display.

20. Diagnostic 0FH -- CMOS RAM power down data retention test

Displays the data contained in the CMOS RAM, writes the pattern 00H, 01H, 02H, CMOS RAM with this pattern, subsequently powering down and powering up the 4500 with this diagnostic still enabled demonstrates if the pattern is preserved and that the battery powered memory back up system is functioning.

21. Diagnostics 10H -- Channel A alignment aid

See Diagnostic 11H.

22. Diagnostic 11H -- Channel B alignment aid

Diagnostic 10H is used for aligning channel A; 11H is used for aligning channel B. These diagnostics display a graticule and a message indicating which channel is being tested. Unlike the other diagnostics, changing the DIP switch LSB (i.e., changing from 10H to 11H or vice versa) causes these tests to measure the channel selected by the DIP switch without the need for depress-ing the reset pushbutton. In these tests; input signals from the front panel BNC are internally disconnected and the offset circuitry generates a ramp applied to the ADC. The output of the ADC is then compared to the theoretical ideal output for the ramp input used and a plot is generated on the CRT.

The plot shows the difference between the theoretical and measured ADC values; therefore, an ideal ADC shows a straight line at zero on the display. When the values are calculated in these tests, more than one acquisition is averaged. These tests allow a resolution of better than one bit as a result. The graticule shown represents one-half bit for each vertical division. Note that these diagnostics are an alignment aid and not generally useful for measuring ADC performance. The display may be entirely offscreen and the ADC may still operate correctly due to its AUTO CAL ability.

23. Diagnostic 12H -- ROM Checksum Test

This diagnostic calculates the ROM checksum and displays it on the CRT. The checksum should be zero.

SPARE COMPONENT RECOMMENDATIONS

The following list shows the components that fail most frequently. These components should satisfy most repair requirements. Consult the factory for recommendations for maintaining multiple systems. Provide a description when ordering parts because the following part numbers may change without notice.

Part Number	Description	Qty.	Comments
2600-0014-10	Relay	2	
1700-0104-10	LF355	1	
1700-0108-10	LM11CLN	1	
1700-0094-10	TDA-1170	1	Mustalsoreplace heatsink
7000-0366-10	Heatsink for TDA-1170	1	
1700-0080-10	CA3086	1	
1700-0081-10	MC1391P	1	
1850-0132-10	10H02	2	
1850-0092-10	AM6688	1	
7000-0125-10	Heatsink for AM6688	1	Must be assembled at Factory
1850-0078-10	100102	1	
1850-0080-10	100114	1	
1700-0032-20	SL3127C	2	
1700-0008-10	CA3049T	1	
2600-0013-10	Relay	2	
1300-0058-10	BFR-96	1	
4600-0016-10	Adjustable, Cap	1	
1000-0024-10	D4858	1	
1700-0099-10	HAI-4605-5	1	
7300-0028-10	6A. Fuse, 3AG.	1	
1400-0039-10	2N4276	2	
1400-0030-10	2N5883	1	
7200-0016-10	Insulator	5	
1300-0054-10	2N6545	2	
1820-0004-10	14012	1	
1700-0086-10	LM324	1	
1700-0096-10	LM358	1	
1200-0031-10	1N4937	2	

CHAPTER 4 CALIBRATION

INTRODUCTION

This chapter provides detailed calibration procedures for the Gould Design and Test Systems Division 4500 Digital Storage Oscilloscope. Many of the procedures set up conditions for those that follow, and some adjustments are interactive. Therefore, the procedures must be followed in sequence.

Do not change any calibration settings if you suspect any part of the 4500 has failed. Changing adjustments may cause other 4500 sections to malfunction, and will make troubleshooting more difficult.

RECOMMENDED CALIBRATION INTERVAL

The 4500 has an AUTO CAL feature that automatically calibrates the ADCs for gain and offset errors. The correction factors currently in use may be obtained from the CAL display that is accessed via the SELF TEST menu. The correction factors have a range of from -128 to +127. When any correction factor becomes greater than +/-100, the AUTO CAL circuitry is approaching the limit that it can correct for.

The Performance Verification Procedure in this manual is a thorough test of the 4500. This procedure is a good indication of the need for calibration, if any.

The system should be calibrated if any of the following conditions exist:

1. If the CAL display, accessed via the SELF TEST menu, shows any correction numbers more positive than +100 or more negative than -100.
2. If the 4500 fails to pass the Performance Verification Procedure.
3. If the 4500 is operated for an accumulated time of more than 1000 hours since the last calibration.
4. If one year has passed since the last calibration.

RECOMMENDED CALIBRATION SEQUENCE

If a complete 4500 calibration is being performed, it is recommended that the circuit boards be calibrated in the following sequence:

1. Power Supply
2. MPU
3. CRT Driver
4. Floppy Disk Interface
5. Sweep and Record
6. Channel A ADC and Attenuator, and External Trigger Attenuator

   The Channel A ADC Calibration Procedure specifies when the Channel A Attenuator and External Trigger attenuator are to be adjusted.

7. Channel B ADC and Attenuator

   The Channel B ADC Calibration Procedure specifies when the channel B attenuator is to be adjusted.

RECOMMENDED TEST EQUIPMENT

A list of recommended test equipment is provided at the beginning of Chapter 2, Performance Verification.

CALIBRATION PROCEDURES FOR MODULE REPLACEMENT

The following procedures provide general guidelines for calibration after a module has been replaced or repaired. These procedures should apply in most cases, but there may be some exceptions that are not covered. If a module has been repaired, recalibration may not be necessary, depending upon the circuitry affected by the repair.

MPU Board

The MPU board can be replaced or repaired without affecting system calibration. There is one adjustment on this board for the CPU oscillator. Although it should not need to be adjusted, it should be checked any time another board is installed. Refer to the MPU Board Calibration Procedure.

Interface Board

The Interface board can be replaced or repaired without affecting system calibration. This board only contains the external interfacing circuitry, therefore, the board does not have to be installed for the system to operate. There are no adjustments on this board.

Floppy Controller Board

The Floppy Controller board can be replaced or repaired without affecting system calibration. This board only contains circuitry used for floppy disk drive operation, therefore, the board does not have to be installed for the system to operate properly. There is one adjustment on this board for the +12 volt power supply used by the disk drive. Although it should not need to be adjusted, it should be checked any time another board is installed. Refer to the Floppy Controller Board Calibration Procedures.

CRT Driver Board

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*** Warning ***
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High voltage is present on this board. Injury or death to personnel could result from contact with this high voltage. Refer to the CRT Alignment Procedures.

The CRT Driver board contains the display generation circuitry and the system operating software. If a replacement board, with a different software revision, is installed there may be some differences in the system operation noticed. However, most revisions are typically created for enhancements to the Self-test Diagnostics, the system operation or to correct software bugs.

The software revision is written on the EPROMs installed in the board and can also be observed in the upper left-hand corner of the MPU/CRT self-test diagnostics display. Your local distributor or factory representative can provide information regarding software changes.

Due to differences in the CRT tube and yoke, it may be necessary to perform a CRT alignment if a board is replaced. Although some of the adjustments may not need to be performed, a complete calibration is recommended to provide the best display. The horizontal and vertical hold pots should always be adjusted in order to prevent the possibility of intermittent loss of display stability. The display INTENSITY control located on the front panel should also be adjust-ed to prevent burning of the CRT face.

All adjustments located on this board affect display integrity only, and repair or replacement should not affect the system operation with the exception of software revisions.

Sweep and Record Board

The Sweep and Record board contains the high-speed memory, and controls many of the recording functions. Proper calibration of this board is critical to system operation. This board should always be completely calibrated any time it is replaced or repaired. A replacement board may operate properly when installed, but an adjustment could be just within operating range and result in intermittent failures.

Improper calibration of the system's clocking circuitry may provide misleading symptoms, indicating improper analog circuitry performance of the ADC boards. Each ADC board provides a slightly different load on the Sweep and Record board clocking circuitry. Therefore, any time another board is installed, it must be recalibrated.

When installing a replacement board, the first step is to perform a complete calibration of the board as described in the Sweep and Record Board Calibration Procedure. Then perform the 33-MHz Alias Test (step 44) of the ADC Calibration procedure. Be sure to check both channels. The only adjustment described in that step that needs to be made is R668. This adjustment should compensate for any differences between Sweep and Record boards.

If the system fails the 33-MHz Alias Test, it may be necessary to perform the other adjustments described in step 44, after rechecking the 100-MHz oscillator on the Sweep and Record board. Once both channels pass the alias test, the Auto Cal and DNL Test (step 51) of the ADC Calibration Procedure should be performed as described. No other part of the system should require calibration.

Attenuator Board

If the Attenuator board is replaced or repaired, the board should be completely calibrated as described in the attenuator board Calibration Procedure. Adjustments for the input capacitance and frequency response are typically not required, but are recommended to assure optimum performance. No other adjustments to the system should be required.

Once the Attenuator board has been calibrated, the self-test diagnostics should be run to verify proper operation. The Auto Cal and DNL Test should be checked as described in step 51 of the ADC Calibration Procedure.

ADC Board

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* CAUTION *
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Always check replacement boards carefully for damaged or bent components prior to installation. The ADC board is a high density board that can be damaged easily. Bent components could cause damage to other system modules.

Jumpers on ADC board determine whether the board is used for channel A or channel B. If necessary, modify the jumpers as shown in Figure 4-1 of the ADC Calibration Procedure. The channel A board provides the circuitry for the external trigger and channel B does not use the circuitry. Always check for correct jumper placement before installing a replacement board.

1. Install the replacement ADC board and connect all of the cables.

2. Power up the system and operate the Self-test Diagnostics. The attenuator's calibration must be matched to each ADC board, therefore, some of the analog tests may indicate out-of-tolerance specifications. If the board does not appear to be recording close to expected results, perform the next step.

3. If necessary, adjust R668 as described in step 42 of the ADC Calibration Procedure. Later in this procedure, R668 will be adjusted accurately.

4. Perform the Attenuator Calibration Procedure as described, except the input capacitance and frequency response adjustments.

5. Perform the 33-MHz Alias Test, (step 44) of the ADC Calibration procedure. The only adjustment that should be needed is R668.

6. Perform the Auto Cal and DNL test as described in step 51 of the ADC Calibration Procedure. The adjustments described in this step should bring the 4500 within specification.

7. Verify that the external trigger circuitry is within tolerance. The test is described in steps 46 through 50. The only adjustment that should be needed is the external trigger balance adjustment (R101) described in step 50.

POWER SUPPLY CALIBRATION PROCEDURE

1. The power supply has ten adjustment potentiometers that set the five power supply voltages and the five overcurrent shutdown values. These potentiometers are accessed at the bottom of the 4500. The location of each potentiometer is printed on the bottom of the power supply. The voltages measured during the calibration procedure are accessed at the edge connectors on the bottom of the motherboard.

2. Remove the bottom cover of the 4500. Set the 4500 POWER switch to ON. Ensure that the line voltage is within 5 percent of the nominal value.

3. From the bottom of the 4500 measure the following nominal voltages on the printed circuit board edge connector and pins specified. Reference Mother Board Assembly Drawing, 0285-0020 for connector location. Adjust the potentiometer specified to set the voltage to the value specified. Connect DVM ground to the common return of the power supply which is the motherboard mounting screw on the left side of the board.

Nominal Voltage	Connector	Pins	Potentiometer	Value
-5.2 V	J3	1 to 8	R87	-5.35 +/-0.02 V
+5.0 V	J3	15 to 18	R129	+5.01 +/-0.05 V
-2.0 V	J3	9 to 12	R141	-2.14 +/-0.02 V
-18.0 V	J7	27 to 28	R64	-18.01 +/-0.05 V
+18.0 V	J7	29 to 30	R63	+18.01 +/-0.05 V

4. The overcurrent shutdown values are set by causing the power supply to output each shutdown current, and then adjusting the potentiometer until shutdown occurs. This adjustment procedure can not be implemented while the power supply is connected to 4500 circuitry and it is recommended that the factory settings not be modified. The nominal voltage of each supply, along with its overcurrent shutdown value and the adjustment potentiometer that sets this value, are listed below for reference.

Nominal Voltage	Overcurrent Shutdown Value	Potentiometer
-5.2 V	16 A	R95
+5.0 V	12 A	R94
-2.0 V	7 A	R96
-18.0 V	4 A	R53
+18.0 V	7 A	R54

MPU CALIBRATION PROCEDURE

1. To adjust the oscillator on the MPU circuit board, place the board on an extender card and switch on 4500 AC power. Monitor U18 pin 12 with a frequency counter. Using a nonmetallic adjustment tool, adjust capacitor C4 to obtain a frequency of 40 +/-0.005 MHz. Determine the range of adjustment within which a stable 40-MHz oscillation is maintained. Leave C4 set in the middle of this stable range. Switch the 4500 power on and off several times and verify the oscillator still oscillates at 40 +/-0.005 MHz.

CRT CALIBRATION PROCEDURE

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* WARNING *
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1. The flyback transformer, located under the aluminum shield that covers the CRT Driver circuit board, and the lead from this transformer to the CRT, contain high voltages. Improper care around these devices could result in electrical shock causing injury or death to personnel.

2. Initiate the CRT alignment test pattern diagnostic by setting the DIP switch on the MPU board to OEH (switches 2, 3, and 4 open and all other switches closed) and depressing the reset pushbutton switch.

3. Set the HOR FREQ and VERT HOLD adjustment potentiometers to obtain a stable display. Rotate each potentiometer clockwise and counter-clockwise until the raster becomes unstable. Determine the range of adjustment required to maintain a stable raster. Leave each of these adjustments set in the center of this stable range.

4. Set the FOCUS control for the sharpest possible display.

5. Set the SIDES control for the straightest possible left and right sides of the display.

6. Set the SIDES BAL control for the straightest possible left and right sides of the display. It may be necessary to readjust the SIDES control for optimum straightness.

7. Set the T&B control for the straightest possible top and bottom of the display.

8. Adjust the T&B TRAP control to obtain the top and bottom of the display as parallel as possible.

****
* CAUTION *
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Do not overtighten the screw holding the yoke to the CRT neck. Failure to heed this caution may crack the CRT neck.

9. Loosen the screw that tightens the deflection yoke to the neck of the CRT. Turn the deflection yoke to obtain the top and bottom of the display as parallel as possible with the transparent CRT window on the front panel. Tighten the screw that fastens the deflection yoke to the CRT neck.

10. Adjust the HOR LIN control for uniform spacing between the vertical lines on the display.

11. Adjust the VERT ON AXIS control for uniform spacing of the horizontal lines on the display.

12. Adjust the VERT PHASE control, WIDTH control, and CRT centering magnets, which are controlled by the two metal tabs on the rear of the deflection yoke, to center and size the display. There should be a 0.3 inch border between the display and the edge of the transparent CRT window on the front panel. If necessary, adjust coil L4 to control the vertical height of the display. Be sure to use a proper size nonmetallic adjustment tool. The tuning slug of this coil is easily broken. Note that moving the centering magnets may affect the sides, top and bottom adjustments; and it may be desirable to readjust the magnets.

13. Adjust the contrast control and brightness control (located on the front panel) for the desired contrast and brightness.

FLOPPY DISK INTERFACE CALIBRATION PROCEDURE

1. The 12 V regulator that supplies power to the floppy disk drive is adjusted in this step. Place probe ground on the negative end of C45, which is located in the lower left corner of this board. Probe the positive end of C45. Adjust R18 for +12.00 +/-0.01 V.

SWEEP and RECORD CALIBRATION PROCEDURE

1. Set an oscilloscope to measure ECL signals by setting both channels to 0.5 V/div with the centerline of the scope representing -1.3 V (ECL threshold).

2. Attach a 500 ohm or FET probe to each of the scope inputs and set the scope input impedance to 50 ohms.

3. Place the Sweep and Record board on an extender card.

4. Depress: MASTER MENU
TRIG SRC, menu key 8
MANUAL, menu key 8

This will prevent the 4500 from taking recordings during the next steps. If the 4500 were allowed to record, small amplitude changes in the 100-MHz oscillator output would be observed, and might be misinterpreted as oscillator instability.

5. Connect a frequency counter to the CLOCK OUT connector on the rear panel. With an oscilloscope, monitor TP21 located near U19F pin 14, with the probe ground connected to TP15. Adjust C102 with a nonmetallic adjustment tool until an oscillation appears on the oscilloscope. With the frequency counter, verify that the oscillator is running at a frequency of 100 +/-0.005 MHz. With the oscilloscope verify that the oscillation is stable with no jitter. There is only a small range of adjustment of C102 where the oscillator will stably oscillate. Adjust C102 so the oscillation is stable. Turn 4500 power off and on several times to ensure the oscillator will power up and remain stable.

6. The differential signal on U18F pins 15 and 9 is the ADC STROBE. This signal goes to both ADC boards, and is buffered and delayed on the ADCs. This signal then returns to the SWEEP and RECORD board as the differential signals A DATA READY from ADC A and B DATA READY from ADC B. Check ADC STROBE for good ECL levels with no jitter on U18F pins 15 and 9, with probe ground connected to TP15. If ADC STROBE has jitter, check the SWEEP and RECORD oscillator for stability; if necessary, readjust C102 (see step 5).

7. Check the differential ECL signal A DATA READY on U1E pins 4 and 5, with probe ground connected to TP12. Verify that A DATA READY has good ECL levels with no jitter. If this signal is not good, adjust R668 on the channel A ADC board. Refer to the ADC Calibration Procedure, 33-MHz Alias Test, step 44; and Data Ready Strobe Adjustment, step 42 for further information on adjusting this potentiometer.

8. Check the differential ECL signal B DATA READY on U1E pins 12 and 13, with probe ground connected to TP12. Verify that B DATA READY has good ECL levels with no jitter. If this signal is not good, adjust R668 on the channel B ADC board. To perform this adjustment, the B ADC board will have to be placed on an extender board, or the channel A ADC board will have to be removed to provide access to R668. Refer to the ADC Calibration Procedure, 33-MHz Alias Test, step 44; and Data Ready Strobe Adjustment, step 42 for further information on adjusting this potentiometer.

9. The next procedure sets the write enable strobes WRA1, WRA2, WRB1, and WRB2. To set these strobes, put the 4500 in the single channel mode, arm it, and have it not trigger. Set the 4500 as follows:

Depress: MASTER MENU
TRC1, menu key 1
A, menu key 2
TRC2, menu key C
OFF, menu key 1

Set: TRIGGER DELAY = 0
PRE TRIGGER and POST TRIGGER SWEEP SPEEDS = 2 uS/div
TRIGGER SOURCE = MANUAL (this was set in step 4 above)
ARM = AUTO

10. Set an oscilloscope to measure ECL signals on both channels, using 500 ohm or FET probes. Set the scope sweep speed to 10 nS/div.

11. Measure testpoint TP3A with scope channel 1, with probe ground connected to TP6. Measure TP3B with scope channel 2, with probe ground connected to TP18. Set up the scope to trigger on channel 1.

12. The signal on TP3A (scope channel 1) should be a 9-nanosecond wide negative going pulse with a 20-nanosecond period. Adjust R109 so the pulse is below ECL threshold (-1.3 V) for 9 nanoseconds.

13. The signal on TP3B (scope channel 2) should be a 40-nanosecond period squarewave. Adjust R115 to center the 9-nanosecond pulse on TP3A (scope channel 1) between the edges of the squarewave on TP3B (scope channel 2). Note that a misadjustment of R115 too far counterclockwise can cause the period of the signal on TP3A to be 40 nanoseconds, rather than 20 nanoseconds.

14. Connect the channel 1 scope probe to TP4A, and probe ground to TP13. Connect the channel 2 scope probe to TP4B, and probe ground to TP14. Adjust R111 for a 9-nanosecond pulse on TP4A. Adjust R110 to center the signal on TP4A within the edges of the signal on TP4B. Refer to steps 12 and 13 above.

15. Connect the channel 1 scope probe to TP1A and probe ground to TP5. Connect the channel 2 scope probe to TP1B and probe ground to TP8. Adjust R47 for a 9-nanosecond pulse on TP1A. Adjust R112 to center the signal on TP1A within the edges of the signal on TP1B. Refer to steps 12 and 13 above.

16. Connect channel 1 scope probe to TP2A and probe ground to TP12. Connect the channel 2 scope probe to TP2B and probe ground to TP12. Adjust R11 for a 9-nanosecond pulse on TP2A. Adjust R113 to center the signal on TP2A within the edges of the signal on TP2B. Refer to steps 12 and 13 above.

18. To adjust the plotter output depress:

MASTER MENU
PLOTTER, menu key A
MAX, MAX, menu key 2

Connect a voltmeter to the PLOT X output on the rear panel. Adjust R65 for 10 +/-0.01 V. Connect the voltmeter to the PLOT Y output on the rear panel. Adjust R66 for 10 +/-0.01 V.

ADC CALIBRATION PROCEDURE

The following nine notes apply to all of the ADC Calibration Procedures.

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* CAUTION *
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1. The high component density on this circuit board requires special care when performing measurements. Use an insulated probe with only a small portion of its tip exposed to avoid shorting adjacent components.

2. References to the TOP, BOTTOM, LEFT, or RIGHT of a component is based on viewing the component side of the circuit board with the board edge connector facing down. References to the OUTSIDE of a component refers to the end of the component facing away from the circuit board. The OUTSIDE designation, in this procedure, refers to placing a probe on a resistor that is mounted on end rather than lying down.

3. Channel A ADC is the one closest to the right side of the 4500; Channel B ADC is the second circuit board in from the right side of the 4500.

4. Currently, there are two different revisions of the ADC circuit board; specifically, ETCH A and ETCH C. Several steps in the alignment procedure require probing various points on the different etch boards. ETCH A boards have the ETCH A designation on the solder side near the edge connector. ETCH C boards have the ETCH C designation on the component side near the top center of the board.

5. The channel A and channel B ADC boards have different jumper connections on their solder sides and are not interchangeable unless these jumpers are modified. Figure 4-1 shows the solder side of the ADC circuit board and which jumper pads are to be connected for the ADC to operate with a particular channel. In Figure 4-1 only those jumpers labeled A should be inserted for channel A operation. Likewise, only those jumpers labeled B should be inserted for channel B operation.

6. When an ADC is being aligned on an extender board, a fan should be set up to blow air along the length of the ADC from the rear of the 4500 toward the front. This fan causes component temperatures to be similar to those when the board is in the card cage, and yields a more accurate alignment.

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* CAUTION *
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7. Power to the 4500 must be turned off when inserting or removing any of the printed circuit boards, or when inserting or removing board connectors as in step 1, Alignment Procedure below.

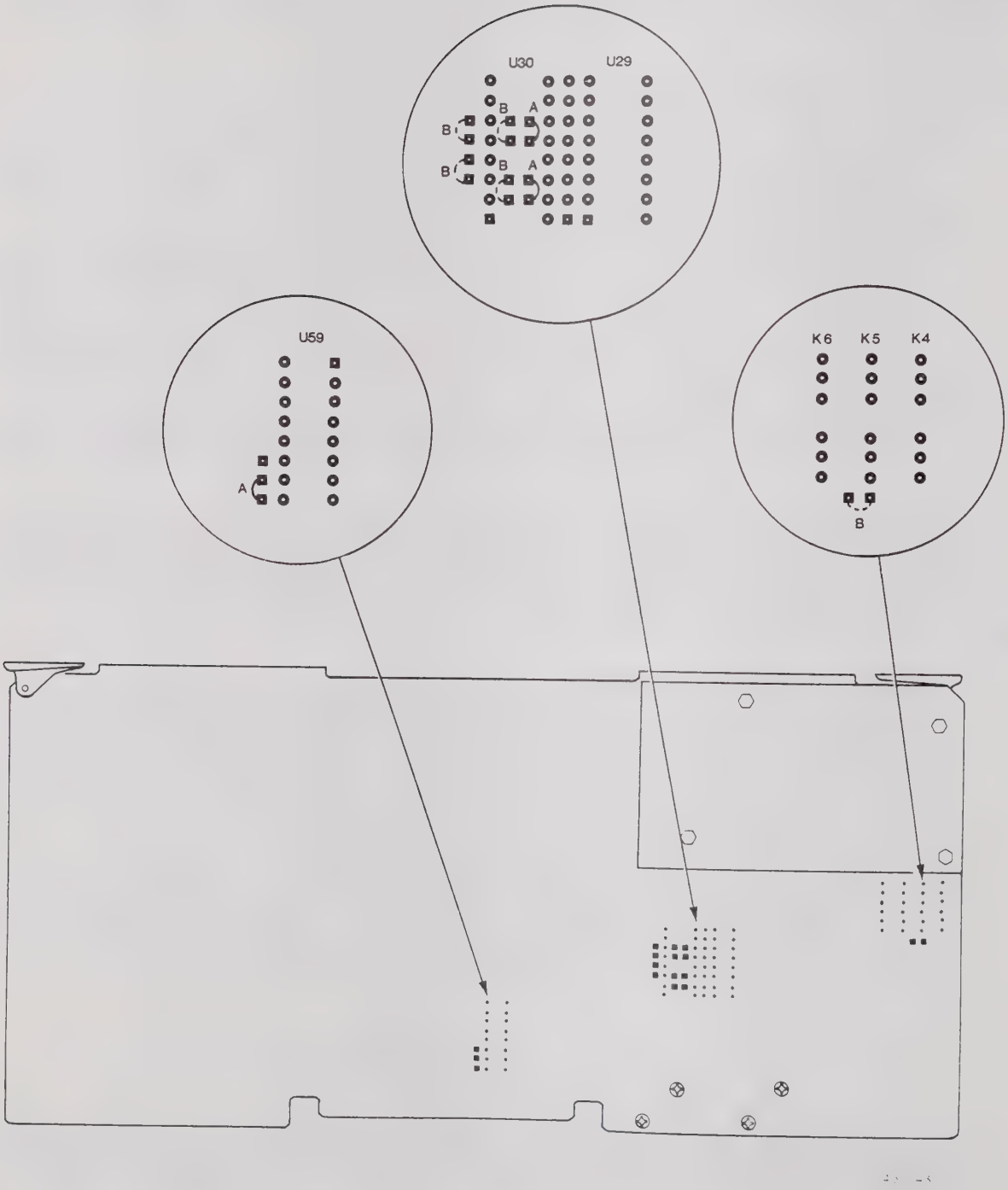


Figure 4-1. ADC Circuit Board Jumpers

8. It is suggested that before a complete ADC calibration according to the following procedure is undertaken, a performance check be done. This may indicate that complete calibration is unnecessary. Overall performance may be evaluated by two tests. These are the 33-MHz Alias Test outlined in step 44, and the CAL numbers check in the SELF TEST menu. If the 33-MHz aliased sinewave is acceptable, then the ADC needs no adjustment except possibly for the auto cal circuitry. By selecting CAL in the SELF TEST menu, the amount of correction currently necessary to bring the ADC into calibration will be indicated on the display. A newly calibrated ADC will show cal correction numbers less than +/-30. The maximum cal correction range available is +127 to -128. The range of numbers shown will indicate how much of the auto cal range has been used and therefore how much is still available. If the numbers are approaching +/-100 then recalibration may soon be necessary. Additional performance verification tests that may be run are the Bandwidth Adjustment test in step 45, and the Trigger Level Adjustment in steps 46 through 50.

9. When measuring signals on the ADC during the alignment procedure, high frequency measurement techniques must be used. This generally means the use of 500 ohm or FET probes, and short ground leads. Familiarity with the measurement of ECL level signals is also necessary. When adjusting the ADC, all probes must be disconnected from circuit points unless called for in the step being executed.

Alignment Procedure Setup

1. At the 4500, set POWER OFF. Remove the input coaxial connector attached to the attenuator and place the ADC to be aligned on an extender board. The coaxial cable carrying the trigger signal from the attenuator is only attached to the channel A ADC and should be left connected. The ribbon cable should also be left connected.

2. On the MPU, set the 8 position DIP switch to hexadecimal 7F by closing the number 8 switch and opening the remaining switches. This action disables the AUTO CAL, which interferes with alignment if left enabled. Set POWER ON at the 4500 (or if power is on, press the RESET switch next to the DIP switch on the MPU board) to start the MPU operating in this mode.

3. Using front panel controls, set the TRIGGER DELAY to 0, the POST TRIGGER SWEEP SPEED to 40 uS/div, the PRE TRIGGER SWEEP SPEED to off (by increasing beyond 10 S/div), the OFFSET VOLTAGES to 0, and SENSITIVITIES to 10 mV/div. Using menu selections, select TRC 1 to be either A for aligning the channel A ADC or B for aligning the channel B ADC. Select TRC 2 to be off. Select TRIG SRC to be MANUAL; this action disables triggering which might cause confusing results during alignment.

Power Supply and Reference Voltage Check

See Figure 4-2 for test and adjustment locations used in the following steps.

1. Ensure the power supply voltages have been adjusted prior to adjusting the ADC. Supply voltages may be checked by placing the digital voltmeter (DVM) probe ground on the top (positive end) of C270 and probing the following edge connector pins. The supply voltages should be within the tolerances indicated below:

ADC Connector Pin	Voltage
30	+5.0 V +/-50 mV
22	-5.2 V +/-50 mV
26	-2.0 V +/-50 mV
72	+18.0 V +/-50 mV
70	-18.0 V +/-50 mV

2. Leave probe ground on the top of C270. Probe the bottom of C270. Adjust R548 for -15.025 V +/-15 mV.

3. Probe the top of C271. Adjust R553 for +15.025 V +/-15 mV.

4. Probe the circuit board feedthrough to the right of C223. Adjust R561 for +10.003 V +/-1 mV. Probe the left end of R333 (Figure 4-3) and verify that it measures -10.003 +/-0.225 V. Probe the left end of R334 (Figure 4-3) and verify that it measures +10.003 +/-0.225 V. These last two measured voltages are not adjustable, but are derived from the reference set by R561. They should be checked for correctness.

See Figure 4-3 for test and adjustment locations used in the following steps.

5. This step adjusts the thermal compensation circuit if it is present. Newer boards have this circuitry removed and this step may be skipped if the components referenced do not exist. When performing this step it is normal for the measured voltage to drift between 50 to 80 mV during adjustment. This changing is especially evident if air flow around the circuit is changed. Probe U23 pin 7. Allow the circuit to stabilize for a few seconds after the DVM is connected. Adjust R528 for +60 mV +/-10 mV. Check the voltage on U23 pin 1, and verify that it is -60 mV +/-10 mV. Probe the wiper of potentiometer R323. Adjust R323 for 0.0 V +/-1 mV.

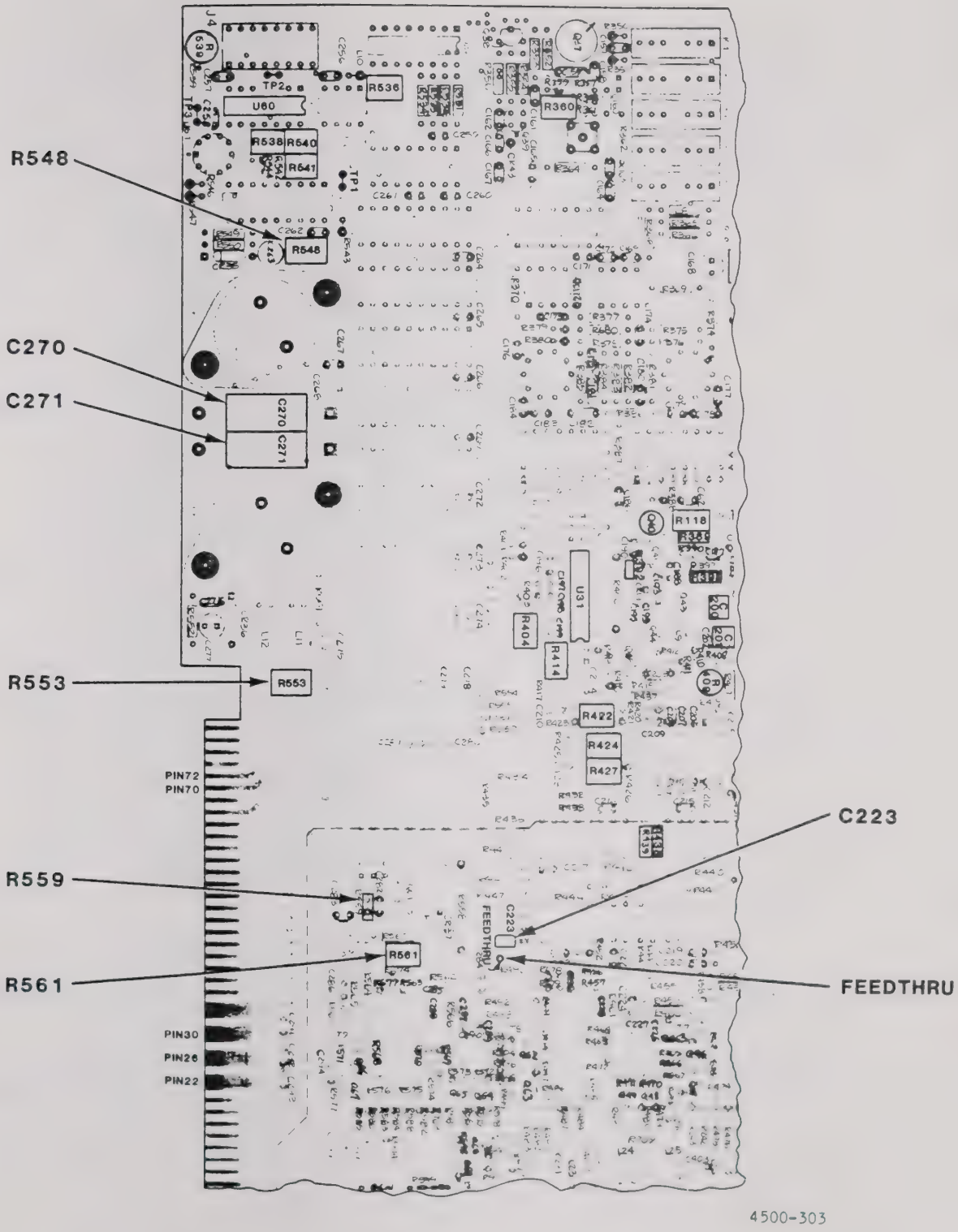


Figure 4-2. Power Supply Adjustment Test Points

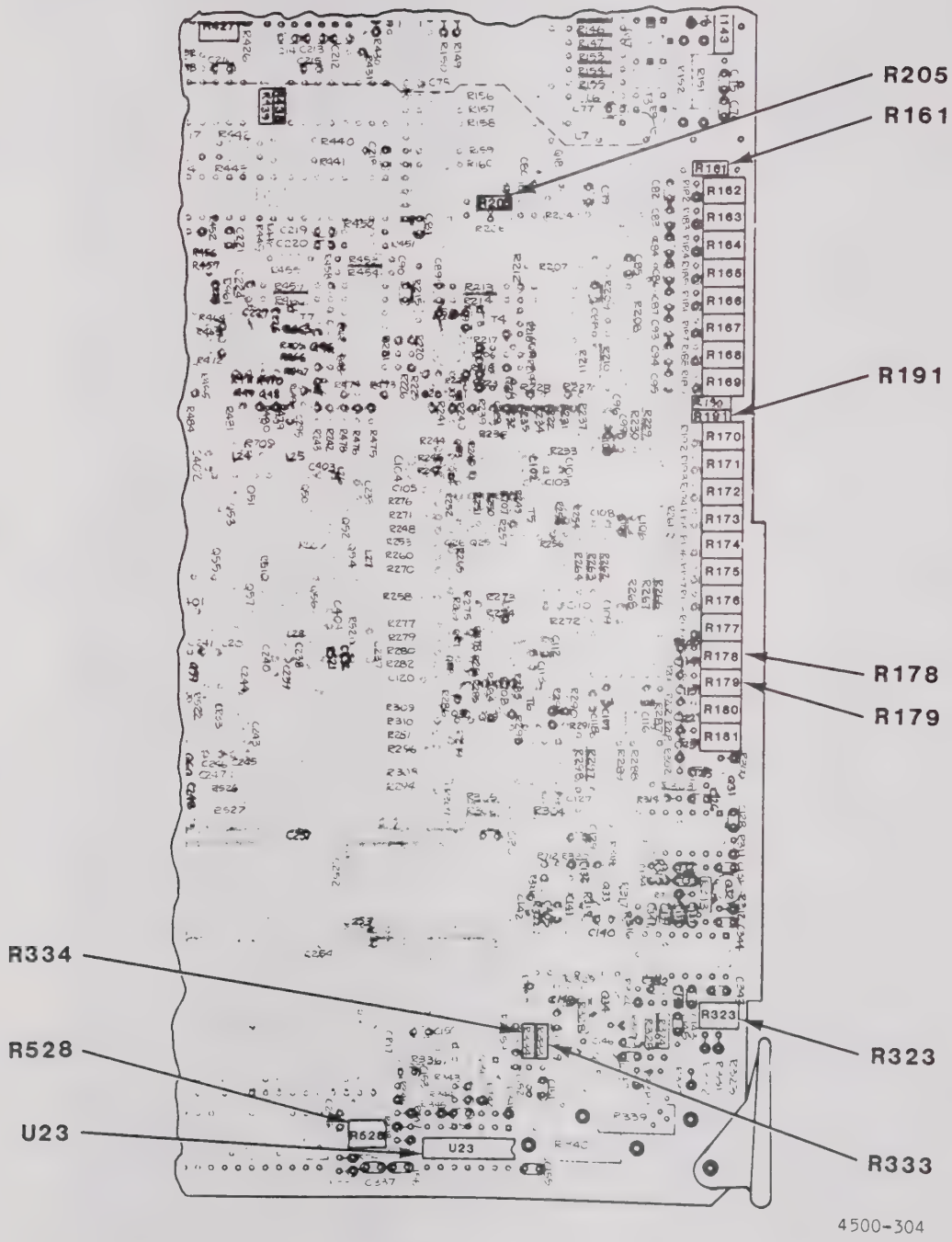


Figure 4-3. Power Supply (Thermal Compensation) Test Points

7. In this step several critical voltages are measured but there are no adjustments to be performed. If the measured values are not within the tolerances specified, a circuit problem is evident and must be repaired for proper operation. Probe the top of R205. The measured voltage must be +11.5 +/-0.4 V. Probe the outside end of R559. See Figure 4-2. The measured voltage must be +6.0 +/-0.3 V. Probe the outside end of CR5. See Figure 4-4. The measured voltage must be -8.8 +/-0.3 V.

8. Probe the top of R161. Adjust R178 for +2.0 V +/-2 mV.

9. Probe the bottom of R191. Adjust R179 for -2.0 V +/-2 mV.

Offset and CAL DAC Adjustment

See Figure 4-5 for test and adjustment locations used in the following steps.

10. Place probe ground on TP1. Set the DIP switch on the MPU board to hexidecimal 0D by closing switches numbered 8, 7, 6, 5, and 2, and opening switches numbered 4, 3, and 1. Press the RESET switch next to the DIP switch to start the CAL DAC adjustment procedure. In this procedure, each time the MASTER menu button is pressed, the CAL DAC changes its output. The output alternates between +10 V and -10 V. These two voltages are used in steps 12 and 13.

11. Probe U60 pin 1. Adjust R540 for 0 +/-100 uV. Probe U60 pin 7. Adjust R539 for 0 +/-100 uV.

12. Probe TP2. Press MASTER until the voltage at TP2 is negative. Adjust R536 for -10.000 V +/-100 uV. Press MASTER to obtain a positive voltage on TP2. Adjust R541 for +10.000 V +/-100 uV. Repeat steps 11 and 12 until all voltages are within tolerance.

13. Probe TP3. Press MASTER to obtain a positive voltage. Set R538 for +2.034 V +/-100 uV. Press MASTER to obtain a negative voltage. The negative voltage should be -2.034 V +/-10 mV.

First Stage Amplifier Adjustment

See Figure 4-4 for test and adjustment locations used in the following steps.

14. Place the probe ground on the top of C270. See Figure 4-5. Set the DIP switch on the MPU to 7F by closing switch number 8 and opening switches 1 through 7. Press the RESET switch next to the DIP switch.

15. Probe the emitter of Q6. See Figure 4-4. Adjust R21 for +7.180 V +/-10 mV.

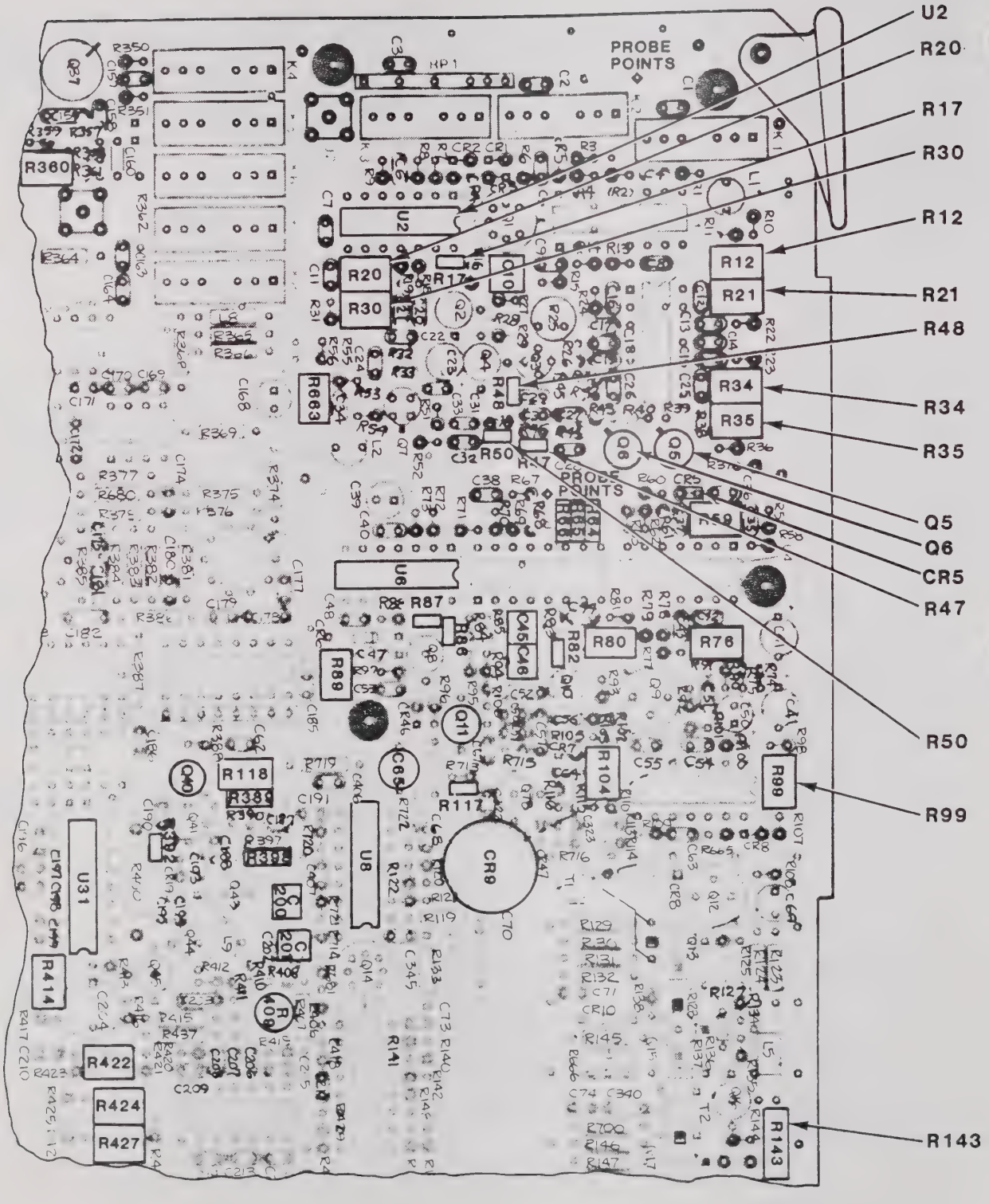


Figure 4-4. Test Point Locations

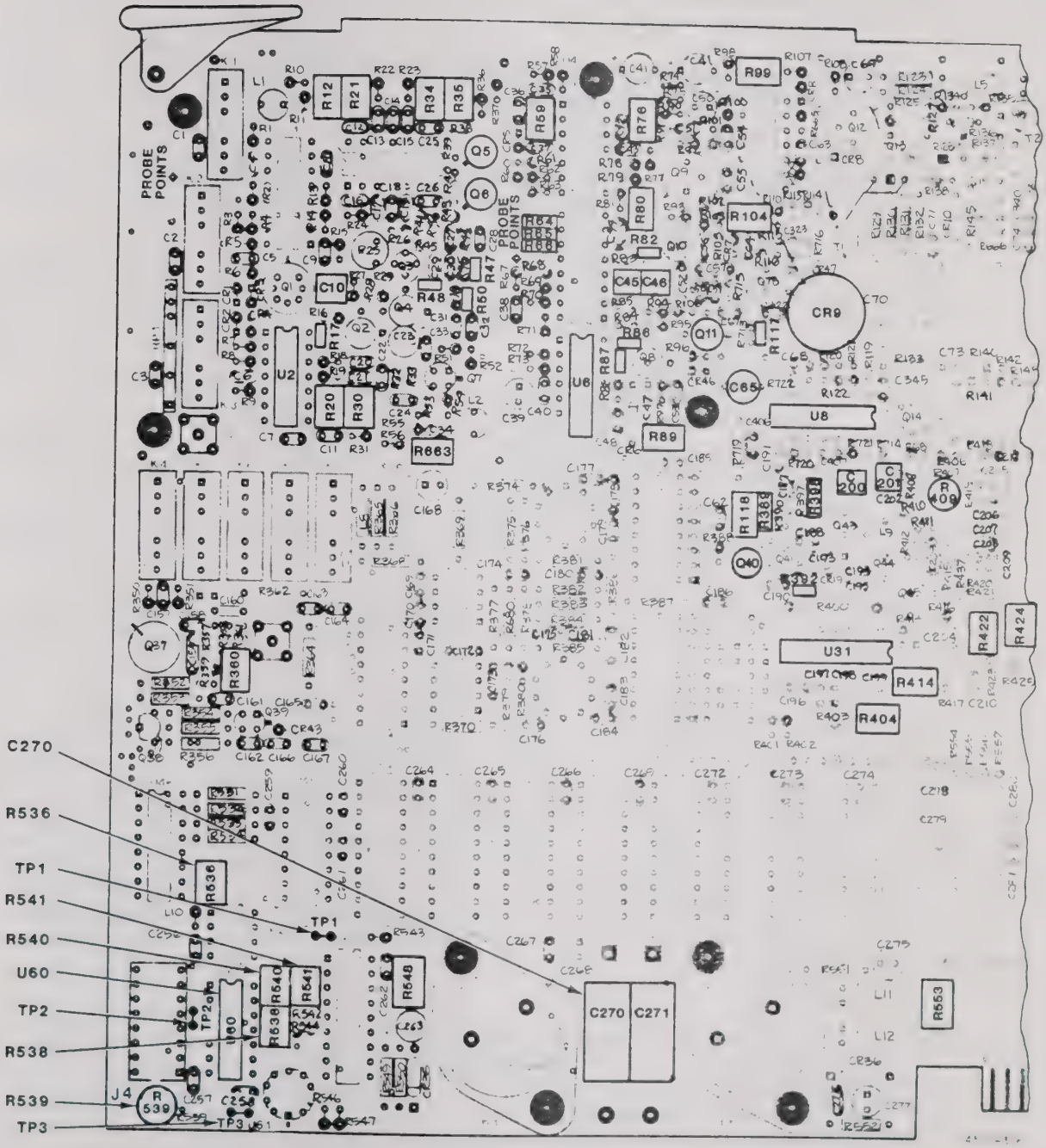


Figure 4-5. Offset and CAL DAC Adjustment Test Points

16. Probe the emitter of Q5. Adjust R34 for +6.390 V +/-10 mV.

17. Move probe ground to the outside end of R47. Probe the case (collector) of Q6. Adjust R12 for +1.200 V +/-10 mV.

18. Move probe ground to the outside end of R17. Probe U2 pin 10. Adjust R20 for 0 volts +/-10 mV.

19. Move probe ground on the top of C270. See Figure 4-5. Probe the outside end of R50. See Figure 4-4. Adjust R35 for +3.960 V +/-1 mV.

20. Probe the outside end of R48. Adjust R30 for 0.0 V +/-1 mV.

TRACK and HOLD CIRCUIT ADJUSTMENT

21. Move probe ground to the left end of R143. Probe the right end of R143. Adjust R99 for -2.600 V +/-5 mV.

See Figure 4-6 for test and adjustment locations used in the following steps.

22. Set an oscilloscope to 50 mV/div, DC input coupling, and 0.1 uS/div, using a 500 ohm or FET probe. Place the scope probe ground on the bottom of R205. Probe the right end of R438. Adjust R104 to obtain the flattest possible trace, disregarding spikes every 200 nanoseconds. Note the spikes are only every 200 nanoseconds if the 4500 sweep rate is set to 40 uS/div as specified in step 2 of this alignment procedure. The spikes should have an amplitude less than 50 mV peak-to-peak. See Figures 4-7, 4-8, and 4-9. If the spikes are greater than 50 mV peak-to-peak perform step 23. If the spikes are between 30 and 50 mV, wait until the 33-MHz Alias Test is performed (step 44). If the results of the 33-MHz Alias Test are not acceptable, then perform step 23 (as noted in the Alias Test) and return to the Alias test.

23. Gently bend the wire stub soldered to the top or bottom lead of CR9 toward the top or bottom of the circuit board, so the peak-to-peak amplitude of the 200-nanosecond spikes referred to in step 22 are minimized. If CR9 does not have a wire stub soldered to one of its leads, a one quarter inch stub (made from a one quarter watt resistor lead) must be soldered to the top or bottom lead to perform this adjustment. Determined by trial which lead to add the stub to so bridge capacitance is balanced and spike amplitude is minimized.

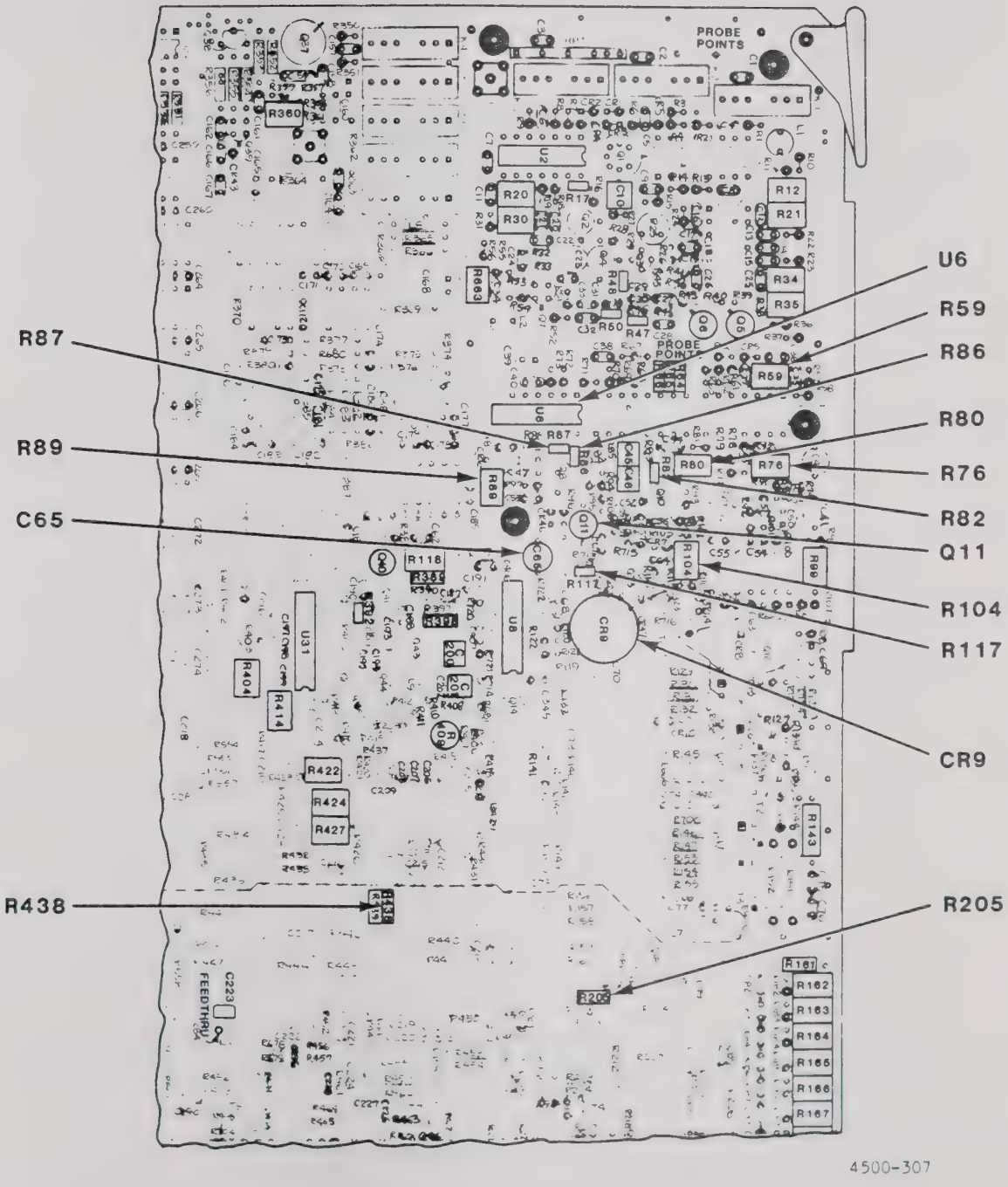
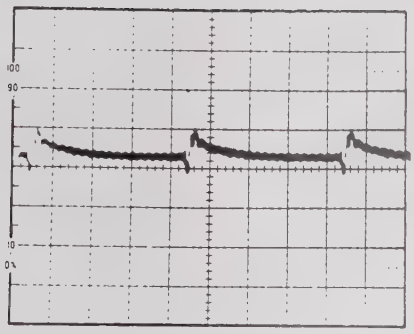
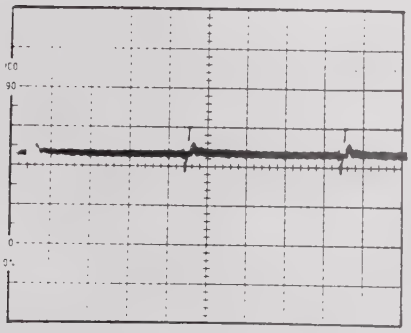


Figure 4-6. Track and Hold Adjustment Test Points



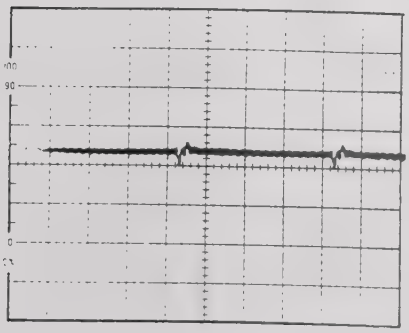
4500-308

Figure 4-7. Track and Hold Waveform Showing Nonflat Performance



4500-309

Figure 4-8. Track and Hold Waveform With 50MV P-P Spikes



4500-310

Figure 4-9. Track and Hold Waveform With 30 MV P-P Spikes

Second Stage Amplifier Adjustment

24. Connect the DVM probe ground to the top of C270. See Figure 4-5. Probe the left side (negative side) of C65. Note that on an ETCH A board it may be difficult to reach the left side of C65. In this event, use the outside end of R82, which is the same circuit point. Adjust R80 for -5.760 V +/-10 mV.

25. Probe the outside end of R87. Rotate R59 fully counterclockwise and then turn R59 clockwise to obtain -0.600 V +/-10 mV. Note that it is possible to continue to turn this potentiometer clockwise and reach another point where the measured voltage is -0.600 V; therefore, the potentiometer is initially turned fully counterclockwise.

26. Place probe ground on the outside end of R86. Probe U6 pin 10. Adjust R89 for 0.0 V +/-10 mV.

27. Place probe ground on the top end of C270. See Figure 4-5. On an ETCH C board, probe the outside end of R117. On an ETCH A board, probe the COLLECTOR (right side) of Q11. Adjust R76 for -1.200 V +/-1 mV.

Third Stage Amplifier DC Adjustment

See Figure 4-10 for test point and adjustment locations used in the following steps.

28. On an ETCH C board probe the outside end of R392. On an ETCH A board probe U31 pin 9. Adjust R404 for 8.27 V +/-10 mV.

29. Probe the emitter of Q40. Adjust R422 for 4.09 V +/-10 mV.

30. Probe U31 pin 13. Adjust R414 for 8.62 V +/-10 mV.

31. Place probe ground on the top of R389. Probe the bottom of R389. Adjust R427 for 2.12 V +/-10 mV.

32. On an ETCH C board, place probe ground on the top end of R398. On an ETCH A board, place probe ground on U8 pin 13. Probe U8 pin 10. Adjust R118 for 0.0 V +/-10 mV.

33. Set an oscilloscope to 50 mV/div, DC input coupling, and 0.1 uS/div, using a 500 ohm or FET probe. Place the scope probe ground on the bottom of R205. Probe the right end of R438. Adjust R424 until the flat part of the trace is at 0.0 volts.

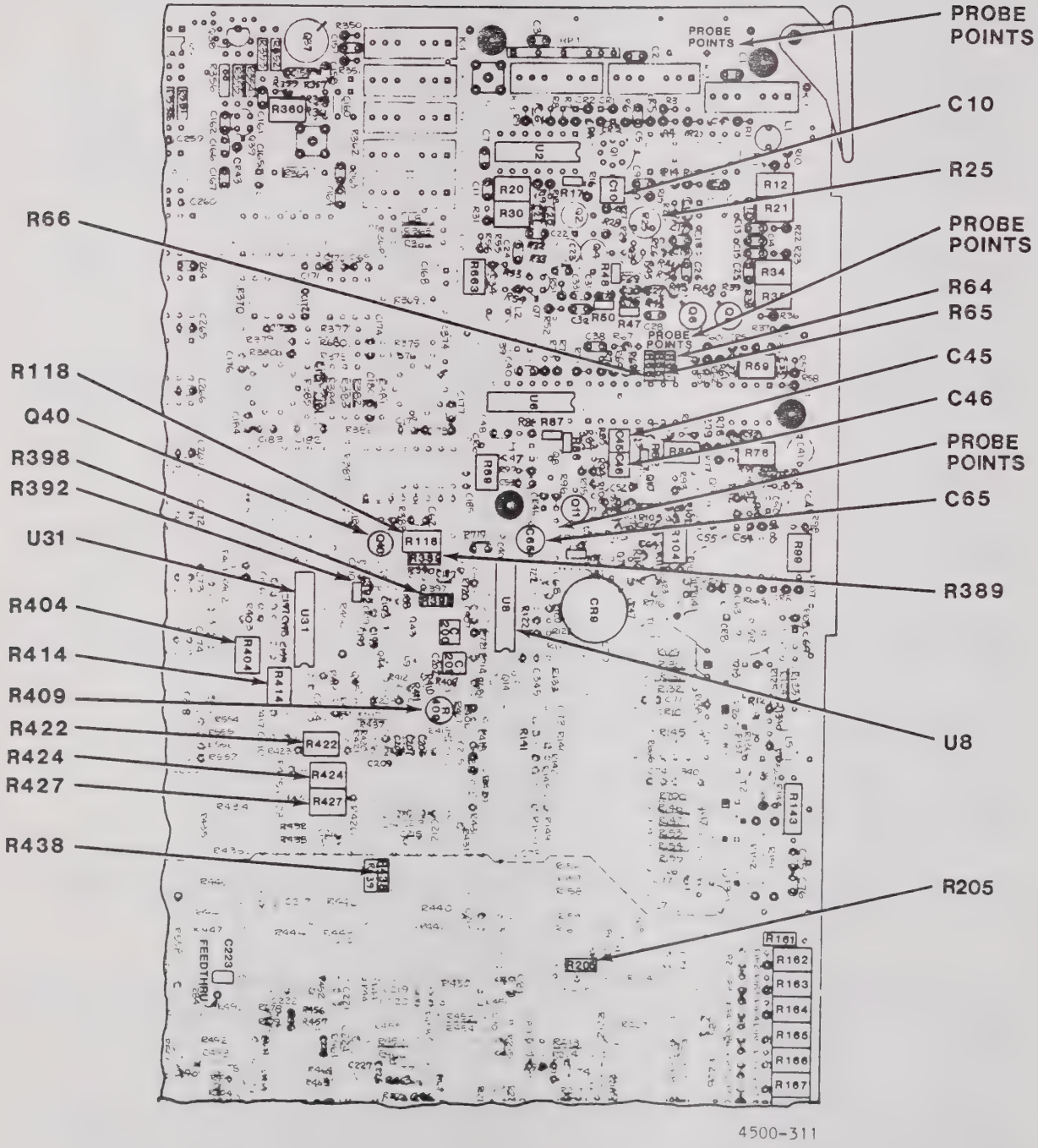


Figure 4-10. Third Stage Amplifier Test Points

34. If the channel A ADC is being calibrated, perform the Channel A Attenuator Calibration Procedure, and the External Trigger Attenuator Calibration Procedure at this time. If the channel B ADC is being calibrated, perform the Channel B Attenuator Calibration Procedure at this time. These procedures may be found in the Attenuator Calibration Procedures section of this manual.

35. In the next steps, the gain of each of the first, second, and third stage amplifiers is set to approximately the desired value using an oscilloscope; the gain is then set more precisely using a DVM. The oscilloscope is used first to ensure that none of the stages are saturating. Connect to the attenuator input (front panel BNC) for channel A or channel B a 1 kHz, 50 mV peak-to-peak, sinewave. Using the CHNL A or CHNL B menu, set the input coupling to AC. Connect a 10 Megohm (X10) probe to an oscilloscope. Connect the scope probe ground lead to the bottom probe point (the point with the round pad) of the probe point pair located at the top left corner of the circuit board. Connect the scope probe tip to the upper probe point (the point with the square pad) of this probe point pair. Adjust the input sinewave for a 100 mV peak-to-peak signal measured at these probe points.

36. Move the probe to the probe point pair located to the left of R64, R65, and R66. Connect probe ground to the round pad and the probe tip to the square pad. Adjust R25 to obtain a 590 mV peak-to-peak sinewave.

37. Move the scope probe ground to the bottom of R205. Connect the scope probe tip to the right end of R438. At this point, there should be a 2.5 V peak-to-peak sinewave with no DC offset. If necessary, adjust R424 for 0 offset and R409 for 2.5 V peak-to-peak.

38. Repeat steps 35, 36, and 37 with a DVM as follows: Ensure the DVM has a frequency response that accurately measures 1 kHz and that the frequency response of the DVM does not change as the DVM range is changed. Set the DVM input coupling to AC. Place the DVM probe on the probe points at the top left corner of the board and adjust the input sinewave for 20 mV rms.

39. Place the probe on the probe points to the left of R64, R65, and R66. Adjust R25 to obtain 117 mV rms.

40. Place the probe ground on the bottom of R205 and probe the right side of R438. Adjust R409 to obtain 0.5 V rms. Set the DVM input coupling to DC and adjust R424 for 0.0 V. Switch the DVM input coupling back to AC and check for 0.5 V rms. Adjust R409 again, if necessary. Repeat step 40 until both values are obtained.

Second Stage Amplifier Rise Time Adjustment

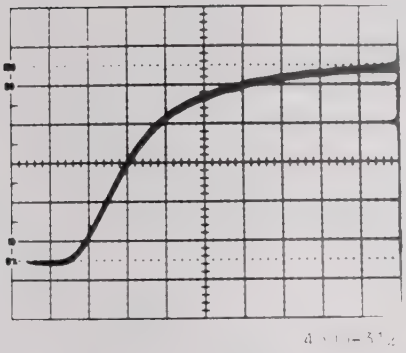
41. Connect a 50 ohm terminator to the 4500 input. Connect the -1 Volt Fast Rise output of a PG506 pulse generator to the 50 ohm terminator and set the pulse amplitude to -1 V. Set the PG506 pulse period to 4 uS. Set the 4500 input coupling to AC, SENSITIVITY to 0.2 V/div, OFFSET to 0 V, and PRE TRIGGER and POST TRIGGER SWEEP speeds to 1 mS/div. Using an oscilloscope with a 500 ohm or FET probe with a short ground lead, connect the probe to the probe points above C65. The probe ground connects to the probe point with the round pad and the probe tip connects to the probe point with the square pad. Set the oscilloscope sweep speed to 10 nS per division and its sensitivity to show a 5 division high trace. Trigger the scope so the rising edge of the waveform at the probe points is visible. Using a nonmetallic adjustment tool, adjust C10, C45, and C46 to obtain the squarest possible pulse corner as the pulse rises to zero volts. There should be no overshoot and the pulse top should be flat. See Figures 4-11, 4-12, 4-13, and 4-14. Change the oscilloscope sweep speed to 5 nS per division and fine tune C10, C45, and C46 to obtain a 7- to 9-nanosecond rise time. This rise time should be measured from one half division above the bottom of the trace to one half division below the top of the trace (the 10% to 90% points). Change the oscilloscope back to 10 nS per division and ensure there is no overshoot as shown in Figure 4-14.

Data Ready Strobe Adjustment

42. See Figure 4-15 for test point and adjustment locations used in the following steps. This step is referenced in the Sweep and Record Calibration Procedure, and if the Sweep and Record board has been calibrated this step will already have been performed. If it has not been performed, it should be done as follows. Set the 4500 PRE TRIGGER and POST TRIGGER SWEEP speeds to 2 uS/div. With a 500 ohm or FET probe, observe the ECL signals on U77 pins 12 and 13. A ground for the probe may be obtained on U73 pin 16. The signals on U77 pins 12 and 13 should be good ECL levels with approximately 50 percent duty cycles. If these signals are not good ECL levels with approximately 50 percent duty cycles, adjust R668 for the best possible signals at these points. All these adjustments are approximate at this point and will be finely tuned later in the procedure.

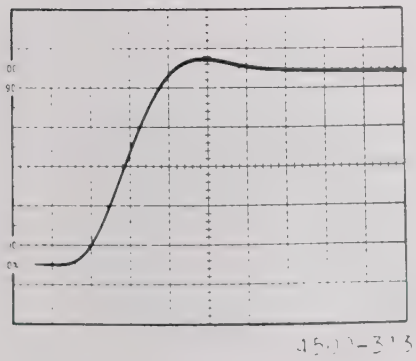
Comparator Adjustment

43. Initiate the Channel A Alignment Aid diagnostic if aligning the channel A ADC, or the Channel B Alignment Aid diagnostic if aligning the channel B ADC. The Channel A Alignment Aid is initiated by setting the MPU DIP switch to 10H (switch 5 opened and all other switches closed) and depressing the RESET switch. The Channel B Alignment Aid is initiated by setting the MPU DIP switch to 11H (switches 1 and 5 opened and all other switches closed) and depressing the reset switch. See the section on 4500 Built-in Manufacturing Diagnostics (Chapter 3) for further information on initiating these aids. The alignment aids bypass all 4500 controls and disconnect all input signals; therefore, the 4500 setup and inputs do not have to be changed.



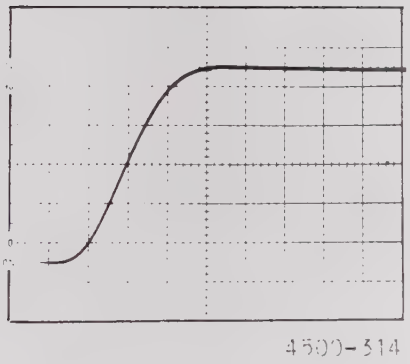
INCORRECTLY ADJUSTED
RESPONSE IS TOO SLOW.

Figure 4-11. Second Stage Amplifier Rise Time Too Slow



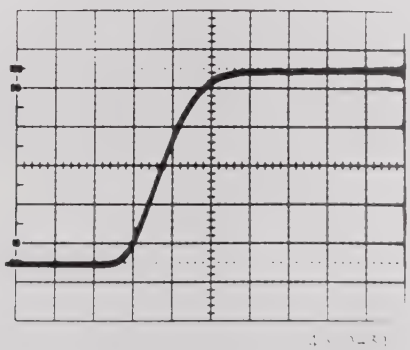
INCORRECTLY ADJUSTED;
RESPONSE SHOWS
OVERSHOOT.

Figure 4-12. Second Stage Amplifier Rise Time Showing Overshoot



INCORRECTLY ADJUSTED;
RESPONSE HAS SLIGHT
OVERSHOOT AND RISE TIME
IS 10.5 NS.

Figure 4-13. Second Stage Amplifier Rise Time With Slight Overshoot



CORRECTLY ADJUSTED;
10% TO 90% RISE TIME
IS 9 nS.

Figure 4-14. Second Stage Amplifier Rise Time Correctly Adjusted

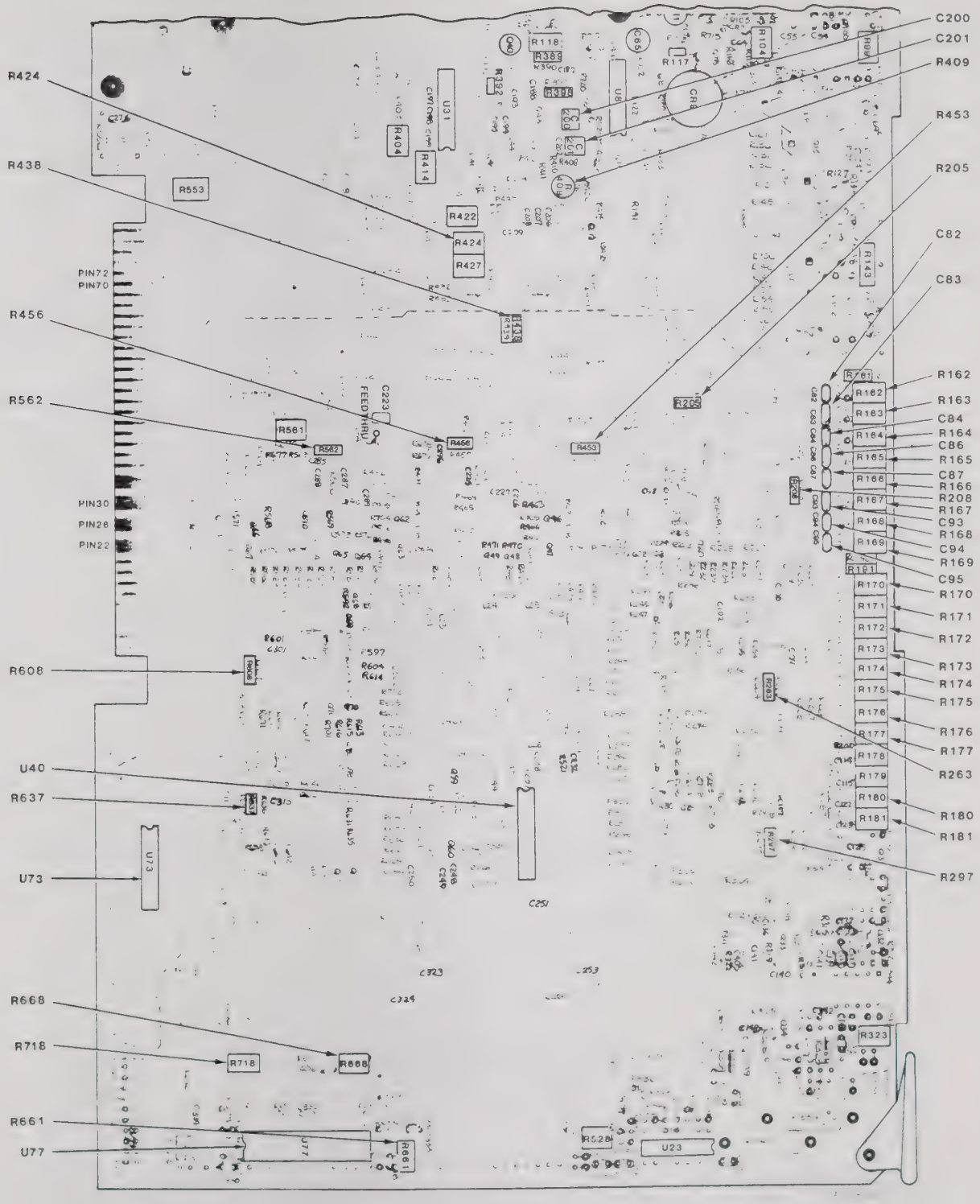


Figure 4-15. Second Stage Amplifier Test Points

The display shows an 8-division high by 8-division wide graticule, and when the ADC is adjusted a waveform will also be shown. There are eight pairs of pots, and two extra pots that must be adjusted. Each pair of pots controls the displayed waveform in one of the horizontal display divisions. One of the pots in each pair controls the vertical position of the waveform in its corresponding division, and the other controls the splitting of the waveform in its corresponding division. Figure 4-16 shows waveform splitting in the third division. The two extra pots control the slope of the waveform sections in all eight divisions. Figure 4-17 shows all eight sections sloped.

On a newly built board that has never been calibrated, the following adjustments need to be made to initially set the potentiometers referenced. On a board that has been operational, or on one that has been factory tested, the initial setting step should not be performed.

Initial settings of all pots must be performed using a DVM. Connect DVM probe ground to the top of C270. See Figure 4-5. Connect the probe to U40 pin 6. Adjust R181 to obtain +0.2 +/-0.1 V. Connect the probe to U40 pin 5. Adjust R180 to obtain +1.1 +/-0.1 V. Next probe across (with the probe ground on one end and the probe tip on the other end) the resistors, adjust the pots, and obtain the voltages shown in the following table.

Probe Across	Adjust Pot	Obtain Voltage
R637	R177	4.00 V +/-10 mV
R608	R176	4.00 V +/-10 mV
R562	R175	4.00 V +/-10 mV
R456	R174	4.00 V +/-10 mV
R453	R173	4.00 V +/-10 mV
R208	R172	4.00 V +/-10 mV
R263	R171	4.00 V +/-10 mV
R297	R170	4.00 V +/-10 mV

Connect the DVM probe ground to the top of C270. See Figure 4-5. Probe the left sides of the capacitors, adjust the pots, and obtain the voltages shown in the following table.

Probe Left Side Of	Adjust Pot	Obtain Voltage
C82	R162	+1.75 V +/-10 mV
C83	R163	+1.25 V +/-10 mV
C84	R164	+0.75 V +/-10 mV
C86	R165	+0.25 V +/-10 mV
C87	R166	-0.25 V +/-10 mV
C93	R167	-0.75 V +/-10 mV
C94	R168	-1.25 V +/-10 mV
C95	R169	-1.75 V +/-10 mV

Initial settings are now complete and a waveform similar to those in Figures 4-16, 4-17, and 4-18 should be displayed. If no waveform is shown then check for 0 offset voltage between the bottom of R205 and the right side of R438 as per step 40 of this procedure. Readjust R424 for 0 offset voltage if necessary.

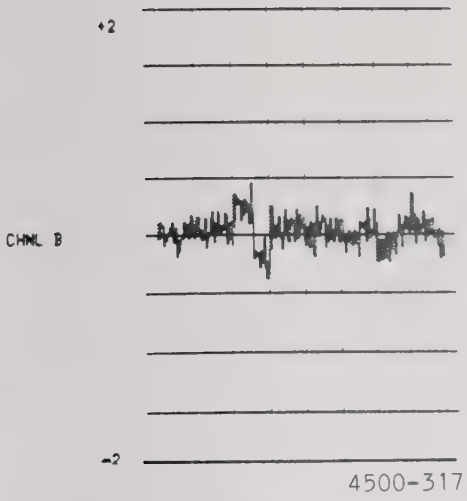


Figure 4-16. Comparator Misadjustment With Waveform Splitting

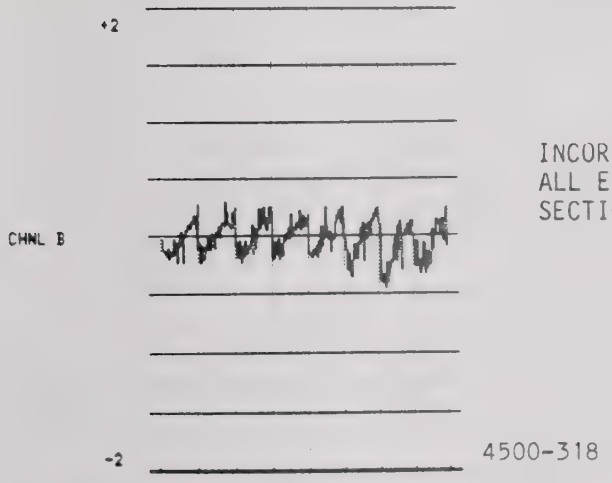


Figure 4-17. Comparator Misadjusted

Figure 4-18. Correct Comparator Waveform

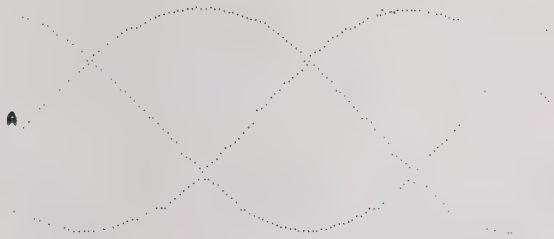
Now that a waveform is displayed, adjust Resistors R169, R168, R167, R166, R165, R164, R163, and R162 so the vertical position of each of the waveform section lies on the zero line of the display, plus or minus 1 division. Adjust R180 and R181 to minimize the sloping of (and any spikes in) the waveform sections. Adjust R170, R171, R172, R173, R174, R175, R176, R177 so the splitting of each waveform section is zero. See Figures 4-16, 4-17, and 4-18. Repeat the above adjustments until all sections are flat and at the zero reference line of the display. Note that a final adjustment to plus or minus one half LSB, which is equivalent to plus or minus one vertical division is acceptable.

33-MHz Alias Test

44. Set the 4500 SENSITIVITY to 0.2 V/div, OFFSET to 0 V, Input Coupling to AC, POST TRIGGER SWEEP Speed to 400 nS/div, PRE TRIGGER SWEEP Speed off, Trigger Source to Auto Trigger on the channel being aligned, and Trace Mode to Dots. Connect a 33-MHz sinewave to the front panel BNC input for the channel being aligned. Set the sinewave amplitude for just less than 4 divisions peak-to-peak on the 4500 display. Adjust the sinewave frequency until stable overlapping sinewaves appear on the display (see Figures 4-19 and 4-20). This is not a display of the actual 33-MHz waveform, but is an aliased sinewave. Adjust R668 in both directions to determine the positions at which the aliased sinewave breaks up. Leave R668 set in the middle of the range, within which the sinewave remains sinusoidal. Use an oscilloscope with a 500 ohm or FET probe and place the scope probe ground on the bottom of R205 and the probe tip on the right side of R438. Adjust C201 to maximize the peak-to-peak amplitude shown on the scope and C200 to minimize the peak-to-peak amplitude shown on the scope. Adjust R661 and R718 for the smoothest aliased sinewave shown on the 4500 display (see Figures 4-19 and 4-20) and adjust C200 and C201 for the smoothest aliased sinewave. Repeat the adjusting of R668, C200 and C201, and R661 and R718 for the best aliased sinewave. If a good aliased sinewave can not be obtained, the diode bridge capacitance may have to be adjusted as outlined in steps 22 and 23.

Bandwidth Adjustment

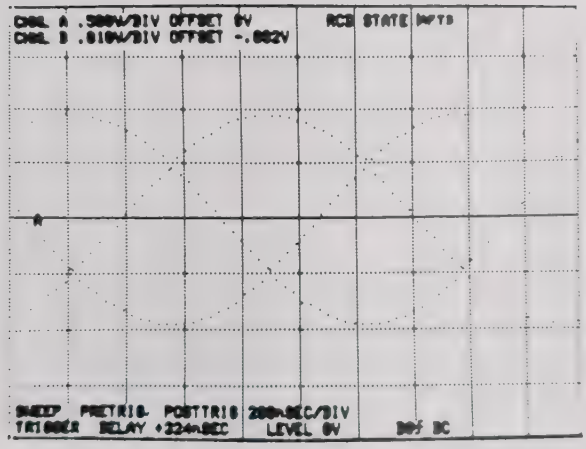
45. Input a sinewave to the 4500 of approximately 660 kHz (1.5-uS period) and adjust the sinewave's amplitude to 6 divisions peak-to-peak as shown on the 4500 display. Change the frequency to 35 MHz without readjusting input amplitude. The 4500 display should now show a sinewave of 4.3 to 5.7 divisions peak-to-peak. If the amplitude is outside these limits, then readjust the pulse response of the input amplifiers as described in step 41.



CORRECTLY ADJUSTED WAVEFORM.

4500-320

Figure 4-19. 33-MHz Alias Test Showing Acceptable Adjustment



IDEALIZED WAVEFORM.

4500-321

Figure 4-20. 33-MHz Alias Test Showing Perfect Adjustment

Trigger Level Adjustment

46. Turn AUTO CAL on by setting the MPU DIP switches to FFH (all switches open) and pressing the MPU RESET switch.

Set the 4500 as follows:

CHANNEL A SENSITIVITY to 1 V/div
CHANNEL B SENSITIVITY to 1 V/div
CHANNEL A OFFSET to 0 V
CHANNEL B OFFSET to 0 V
POST TRIGGER SWEEP speed to 20 uS/div
PRE TRIGGER SWEEP speed off
TRIGGER DELAY to 0 S
TRIGGER LEVEL to 0 V
Input coupling to AC
Trigger coupling to AC
Trigger slope to POS
Trigger source to A AUTO (or to B AUTO if adjusting the channel B ADC)

In this procedure the major cursor is used to measure the trigger level at the trigger point. Select the F(CRSR) menu, then select the T(M-T) function. Set the major cursor position using the MAJOR CURSOR rocker switch so the T(M-T) readout located near the major cursor line on the display reads 0. This action sets the major cursor on the trigger point of the display, which will be located one division in from the left side of the display screen. Using the F(CRSR) menu, select the V(M) function. With the major cursor now set on the trigger point, the cursor V(M) readout will show the trigger voltage.

47. See Figure 4-21 for test point and adjustment locations used in the following steps. Put a 500-Hz, 8 V peak-to-peak triangle wave into the front panel BNC input of the channel being adjusted. A ramp that goes through -3 V and +3 V should appear crossing the screen. Adjust R360 so the V(M) readout is 0 +/-0.2 V. Change the trigger level to +3 V and note the V(M) readout value. Set the trigger level to -3 V and note the V(M) readout value. Adjust R360 so the first V(M) readout value is below +3 V the same amount as the second V(M) readout value is above -3 V. This adjustment sets the offset of the trigger amplifier. Adjust R663 so the V(M) readout is +3 +/-0.2 V when the trigger level is set to +3 V and so the V(M) readout is -3 +/-0.2 V when the trigger level is set to -3 V. R663 adjusts the gain of the trigger amplifier. Both R360 for offset and R663 for gain may have to be adjusted again to achieve these two values.

48. Change the trigger slope to NEG. When the trigger level is set to +3 V, the V(M) reading should be +3 V +/-0.2 V. When the trigger level is set to - 3 V, the V(M) reading should be -3 V +/-0.2 V.

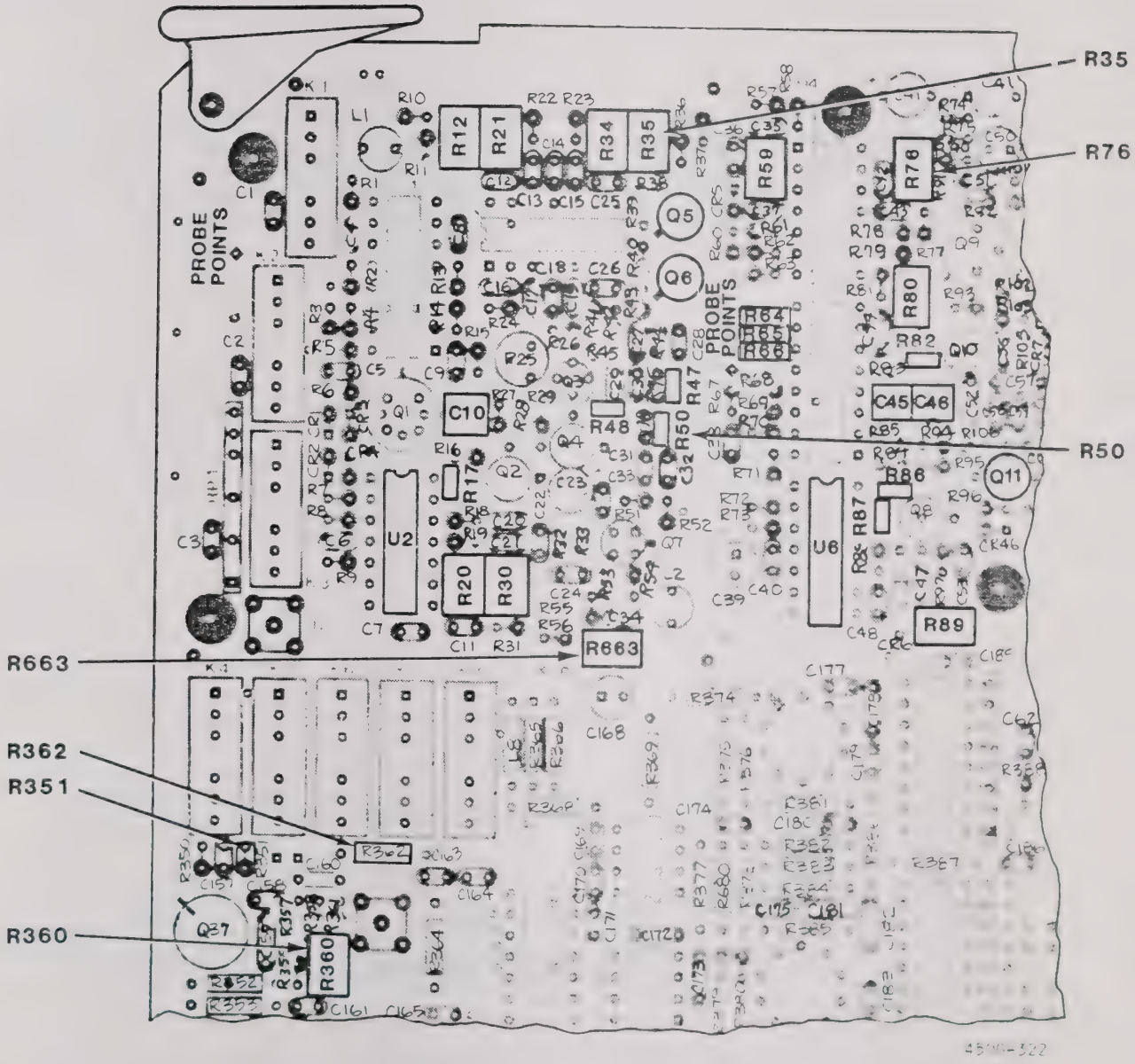


Figure 4-21. Trigger Level Test Point and Adjustment Locations

49. Change the trigger slope to ENT BAND. The V(M) reading should switch between +3 V +/-0.2 V and - 3 V +/-0.2 V. If one of these two values is out of tolerance, adjust R360 (trigger amplifier offset) to bring both within tolerance. This action sacrifices some accuracy on POS or NEG slope triggering to yield better accuracy on ENT band triggering and a better compromise on overall trigger level accuracy.

50. Perform this step only if the channel A ADC board is being calibrated. Connect the input signal simultaneously to the front panel External Trigger BNC input and to the Channel A input BNC connector. Using the TRIG SRC menu set the trigger source to EXT. Verify that the V(M) readout is +3 +/-0.2 V when the trigger level is set to +3 V, and that the V(M) readout is -3 +/-0.2 V when the trigger level is set to -3 V. If necessary, adjust the trigger balance potentiometer (R101) on the Attenuator board to achieve these readings.

AUTO CAL and DNL Tests

51. To further verify ADC performance, the AUTO CAL self test and the DNL self tests should be performed. The AUTO CAL self test indicates the amount of correction required for the ADC input amplifiers to have the proper gain and offset. The channel A and channel B DNL tests show an indication of the differential nonlinearity of these two ADCs.

To initiate the AUTO CAL self test depress:

MASTER MENU
TEST, menu key C
CAL, menu key 8

The CAL correction factors will be displayed as shown in Figure 4-22.

An ADC, when first calibrated, should exhibit all its CAL correction factors in the range of 0 to +/-30. This test should be performed with the 4500 covers in place, and with the unit operated long enough to reach a stable operating temperature.

If any offset correction factor is greater than +/-30, lift the 4500 top cover and adjust R76 on the ADC board with the out of range offset correction factor. This adjustment may be reached with the ADC boards in place and operating. The correction factors should be observed during adjustment and minimized.

If any gain correction factor is greater than +/-30 then adjust R409 (see Figure 4-15) on the ADC board needing adjustment. R409 is not accessible while the ADC is in place. If R409 needs adjustment, the 4500 will have to be powered down, the ADC removed, R409 adjusted a small amount, and the ADC and the top cover replaced.

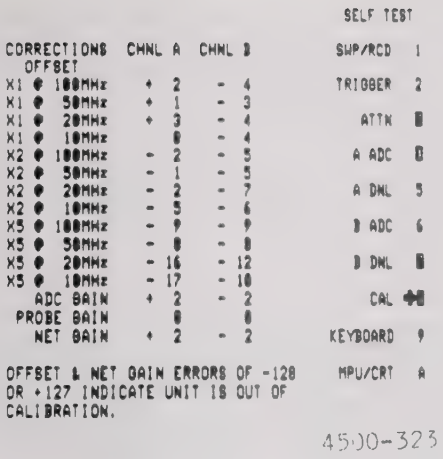
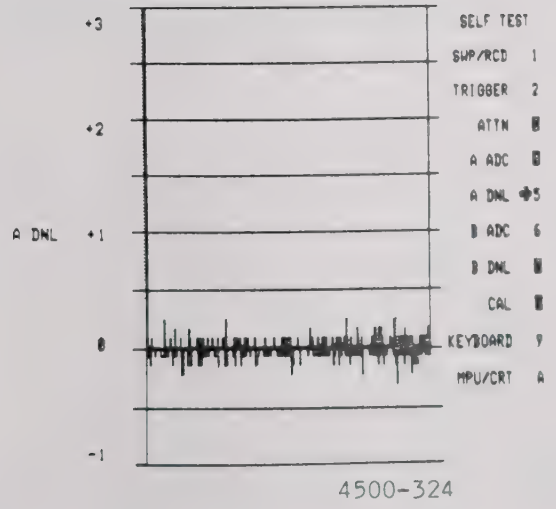


Figure 4-22. CAL Correction Factors Display



ACCEPTABLE RESULT.
NO SPIKE GREATER
THAN +/-1 DIVISION.

Figure 4-23. DNL Test (Slow Version) Correct Waveform

After the gain or offset is changed, observe the correction factors for a few minutes as they stabilize. Readjust R76 or R409 as necessary.

To terminate the AUTO CAL display depress:

HALT, menu key C

The A DNL self test should now be initiated. From the SELF TEST menu depress:

A DNL, menu key 5

The display (see Figure 4-23) shows a histogram of the differential nonlinearity of the ADC for channel A, averaged over a large number of acquisitions.

There are two software versions of this test. In some 4500s (software versions 3.4 and earlier), the DNL test is performed continuously, with the results appearing on the display approximately two times a second. In other 4500s (software versions 4.0 and later), the test is performed once, each time the A DNL key is depressed. The result takes approximately 12 seconds to appear on the display. Figure 4-23 shows an example of the slower version of the test. In the faster version, less averaging is done and more noise (peak-to-peak variation) is apparent in the result. In the slower version more averaging is done and the result shows less peak-to-peak variation. The DNL test is designed to ensure a differential nonlinearity of +/- one half LSB.

In the fast version, an acceptable result shows no more than two amplitude peaks greater than +/-1 division at any one waveform point within five successive tests.

In the slow version, an acceptable DNL result shows a histogram on the zero line +/-1 division. There should be no amplitude peaks greater than +/-1 division.

Next perform the B DNL self test. From the SELF TEST menu depress:

B DNL, menu key 7

Interpret the results as discussed above.

If the channel A or channel B DNL test fails, check that there is good electrical contact between the aluminum shield that is mounted to the back of the ADC board that fails the test, and the spring metal tab that is mounted to the chassis next to the ADC board card guide. If there is good contact, then the problem is most likely the adjustment of the track and hold circuitry.

If necessary, repeat steps 22 and 23.

INPUT and EXTERNAL TRIGGER ATTENUATORS CALIBRATION PROCEDURES

1. The following procedures are used to adjust the attenuators for channel A, channel B, and the external trigger input. These three attenuators are independent; therefore, individual adjustment of one does not affect the others. If one of the channel or trigger attenuators is not to be adjusted, disregard the associated steps.

To access the Attenuator board for adjustment, remove the four screws that attach the front panel bezel to the front casting. When the screws have been removed, the front bezel assembly may be tilted forward to access the adjustments. Ensure that only an insulated adjustment tool is used, as it is easy to short circuitry on the attenuator board to the metal access panel.

Channel A or Channel B IP BALANCE Adjustment

2. Set the channel A or Channel B (whichever channel is being aligned) sensitivity to 0.001 V/div. Connect DVM probe ground to the outer shell of the front panel BNC connector for the channel being aligned. Connect the probe to the inner conductor of the same BNC connector. Measure the DC voltage present on the BNC connector and adjust the IP BALANCE control (R39 for channel A or R86 for channel B) for 0.0 V +/-100 uV. This measurement is extremely sensitive to electromagnetic interference. Static discharge caused by the moving of feet or clothing may result in variations in DVM readings that exceed 100 uV. These variations can be minimized by using a shielded cable on the DVM and reducing body motion while observing the settling of the DVM reading. When this adjustment has been performed it should be verified by setting the trigger source, using the TRIG SRC menu, to either A/AUTO or B/AUTO. Depress AUTO ARM. Short the input BNC connector for the channel being aligned, with a BNC shorting plug or 50 ohm terminator. There should be no movement of the trace as the input is shorted and opened. If necessary, readjust the IP balance control of the channel being calibrated.

Channel A or Channel B OP BALANCE Adjustment

3. See Figure 4-21 for ADC test and adjustment locations. Disconnect the coaxial cable from the attenuator channel being aligned to the ADC. Place DVM ground on the top of C270. With the DVM, probe the outside end of R50 on the ADC board associated with the channel being aligned. Verify a voltage of +3.96 +/-1 mV. If necessary, adjust R35 on the ADC board to achieve this voltage. Now connect the coaxial cable from the attenuator to the ADC. The voltage on the outside end of R50 on the ADC board should be +3.96 +/-1 mV. If it is not, adjust the OP BALANCE control on the attenuator for the channel being aligned (R28 for channel A or R74 for channel B), so +3.96 +/-1 mV is obtained. The voltage should remain constant while the coaxial cable is connected or disconnected.

External Trigger TRIGGER BALANCE Adjustment

4. Ensure the external trigger attenuator output coaxial cable is plugged into connector J3, the trigger input connector, on the channel A ADC board. On the channel A ADC board, place probe ground on the outside end (the end away from the circuit board) of R351. This is a 1 Megohm resistor near the left edge of the ADC circuit board below relay K5. Probe the left end of resistor R362. This resistor is located below relay K7. Using the TRIG SRC menu select EXT (external trigger). With no signal applied to front panel trigger input BNC connector, adjust the TRIGGER BALANCE control R101 for 0.0 V +/-100 uV.

5. The following steps require a pulse generator that generates pulses that are flat to 0.5% or less. A Tektronix PG506 is recommended. The PG506 has two fast rise outputs and a high amplitude output. The pulses from these outputs go to either a positive or negative voltage level and then back to ground. The flat part of these pulses are at ground. This zero voltage level portion of the waveform should be used in these adjustment procedures.

6. The following steps adjust the frequency compensation and the input capacitance of the amplifiers. The input capacitance adjustments set the input capacitance to 30 pF. When adjusting the input capacitance, a calibrated 30 pF input standardizer (part no. 0285-0109-10) is driven by a pulse generator, and the attenuator is adjusted to achieve a square pulse.

Channel A or Channel B AC/DC Control and I/P CAP X1 Adjustment

7. Connect a 50 ohm terminator to the 4500 front panel BNC input connector. Use a Tektronix PG506 pulse generator, and use the PG506 fast rise output that goes from a negative voltage to ground. Connect this output to the 50 ohm terminator. Set the PG506 to output voltage to approximately 100 mV peak-to-peak, and its period to 100 mS. Adjust the 4500 SENSITIVITY to 0.01 V/div, OFFSET to 0, PRE TRIGGER and POST TRIGGER SWEEP speeds to 20 mS/div, and input coupling to DC. Using the TRIG SRC menu select A/AUTO if calibrating channel A, or B/AUTO if calibrating channel B. Depress AUTO ARM. Adjust the AC/DC control (R18 for channel A or R82 for channel B) to obtain the squarest possible pulse corners on the 4500 display as the pulse rises to zero from its negative level. Replace the 50 ohm terminator with the RC input standardizer. Change the PRE TRIGGER and POST TRIGGER SWEEP speeds to 20 uS/div. Change the PG506 period to 100 uS. Adjust the I/P CAP X1 adjustment (C10 for channel A or C42 for channel B) to obtain the squarest possible pulse corners.

Channel A or Channel B COMP X10 and I/P CAP X10 Adjustment

8. Remove the RC input standardizer and place the 50 ohm terminator on the channel BNC input. Change the 4500 SENSITIVITY to 0.1 V/div. Leave the PRE TRIGGER and POST TRIGGER SWEEP speeds at 20 uS/div. Set the PG506 to output approximately 1 V peak-to-peak and 100 uS period. Adjust the COMP X10 control (C7 for channel A or C39 for channel B) to obtain the squarest possible pulse corners as the pulse rises to zero from its negative level. Replace the 50 ohm terminator with the RC input standardizer. Adjust the I/P CAP X10 adjustment (C5 for channel A or C37 for channel B) to obtain the squarest possible pulse corners.

Channel A or Channel B COMP X100 and I/P CAP X100 Adjustment

9. Remove the RC standardizer and place the 50 ohm terminator on the BNC input of the channel being adjusted. Change the 4500 SENSITIVITY to 1 V/div. Use the high amplitude output of the PG506 and set the output voltage to its maximum (approximately 5 V peak-to-peak). Adjust the COMP X100 control (C16 for channel A or C48 for channel B) to obtain the squarest possible pulse corners as the pulse rises to zero from its negative level. Replace the 50 ohm terminator with the RC input standardizer. Adjust the I/P CAP X100 adjust-ment (C12 for channel A or C44 for channel B) to obtain the squarest possible pulse corners.

External Trigger COMP and I/P CAP Adjustment

10. To adjust the trigger attenuator frequency compensation, use an oscilloscope with its probe compensated to show a square response to a squarewave input. On the channel A ADC board (into which the trigger output signal coaxial cable is connected) attach the scope probe ground to the outside end of R351. Attach the scope probe tip to the left end of R362. Set either of the PG506 fast outputs to put out approximately 300 mV peak-to-peak. Set the PG506 period to 100 uS. Connect the 50 ohm terminator to the 4500 front panel trigger input. Connect the PG506 output to the 50 ohm terminator. Using the TRIG SRC menu select EXT (external trigger). Set the oscilloscope to 50 uS/div and 20 mV per div. Adjust the trigger COMP adjustment (C74) to obtain the squarest possible squarewave. Replace the 50 ohm terminator with the RC input standardizer. Adjust the trigger I/P CAP adjustment (C73) to obtain the squarest possible pulse corners.

CHAPTER 5 THEORY OF OPERATION

INTRODUCTION

The following paragraphs describe the 4500 Theory of Operation at the functional signal flow level by referring to the block diagram, Figure 5-1. Following this description, each board is described in detail at the component level referring to the appropriate schematic in Chapter 6.

4500 DIGITAL OSCILLOSCOPE BLOCK DIAGRAM DESCRIPTION

The following block diagram shows the major system components and the passage of data among them. Not shown is the control of the components which is effected from the MPU board to the ADC board, the Sweep and Record board, the Front Panel, the Floppy Disk Interface board, and the I/O Options board via the microprocessor bus.

4500 Overview and Signal Processing

The Gould 4500 is a dual-channel, digital-storage oscilloscope containing two independent 8-bit analog-to-digital converters capable of sampling data at frequencies up to 100 MHz. This section describes the theory of operation of the 4500 by following the processing of the analog inputs through the 4500 to their display on the CRT screen. Following this, other aspects of operation are described.

Signal Input and Analog Steps

The analog signal to be measured, enters the 4500 through a BNC connector on the front panel; is either AC or DC coupled; is divided in a programmable attenuator by 1, 10, or 100; and then has subtracted from it an offset voltage. These steps are accomplished on the Attenuator board, and there are independent circuits on this board for channels A and B. The offset voltage, subtracted from each channel input signal, is generated by a digital-to-analog converter located on the ADC board for each channel.

The analog signal from each channel is applied to an associated ADC board. On the ADC board, the signal is voltage divided by a 1, 2, or 5 programmable attenuator and applied through a track and hold circuit to the input of the analog-to-digital converter.

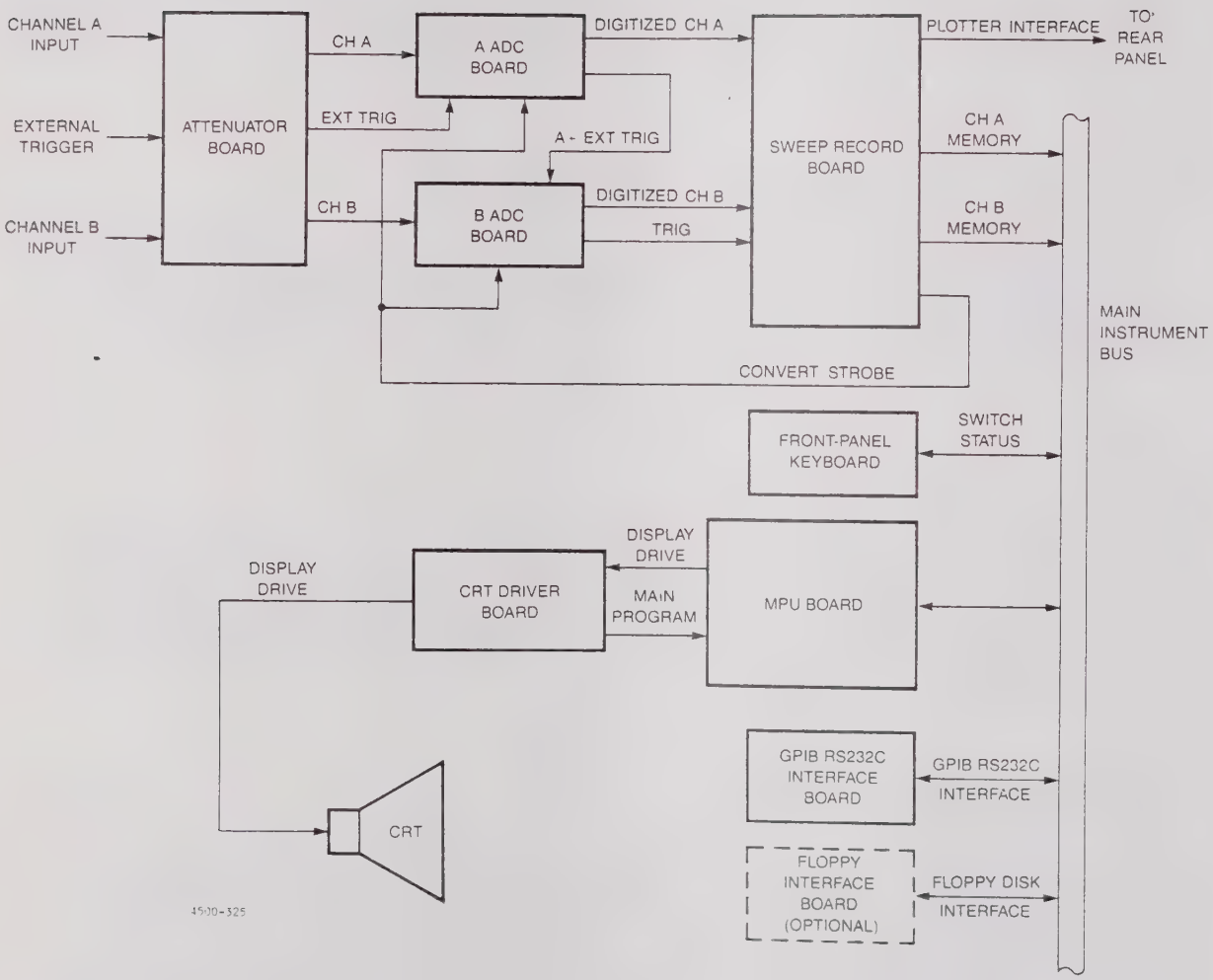


Figure 5-1. 4500 Block Diagram

Signal Input and Digital Steps

When the ADC board receives the Convert Strobe signal from the Sweep and Record board, the track and hold goes into the hold state. The dual rank ADC then digitizes the voltage on the hold capacitor. When the 8-bit digital result is ready, the ADC sends it to the Sweep and Record board in the form of differential ECL signals. A "data ready" strobe is also sent at this time to the Sweep and Record board. The data at this point is Gray coded in the high order 4 bits and folded binary in the low order 4 bits.

The Sweep and Record board contains two high speed memories to store data from each channel. Each memory has storage for 1000 8-bit bytes, however these high speed memories can both be set up to record from the same (channel A or channel B) ADC. This allows a memory length of 2000 samples when only one channel is used.

When the acquisition of data stops (refer to **Time Base Control** below), the microprocessor reads the data from the high speed memories, converts it to 2's complement binary, and stores it in the lower speed memory on the microprocessor (MPU) board.

An exception to this is when the high speed DMA output is selected to be active. In this case, the processor does not transfer the acquired data to the MPU board memory, but instead activates the DMA circuit on the Interface Option (I/O) board. This circuit either transfers digital data to the direct access DR-11B interface connector, on the rear panel; or analog data, reconstructed by a DAC, to the AVERAGER OUT BNC connector on the rear panel. In either case, the data is translated from the Gray code/folded binary to unsign-ed binary (00000000 represents the lowest voltage, and 11111111 represents the highest voltage) during these transfers.

Processing and Display of Acquired Data

The microprocessor either transfers the data from the Sweep and Record board directly into the microprocessor memory (MPU RAM), or it adds the data to the previous contents of this RAM to implement signal averaging. Along with the waveform sample values, the processor maintains waveform acquisition parameters in the MPU RAM. These parameters include:

- the length of the acquisition (1000 or 2000 samples),
- the pretrigger and postrigger sample rates,
- the trigger delay (time of the trigger event relative to the stored waveform samples),
- the attenuation and offset voltage,
- the number of averaging sums (if averaging was selected).

This information is used to adjust the waveform to the scale of the graticule before the waveform is displayed. If the scale of the graticule is changed, for example by changing sensitivity or sweep speed, the waveform is redisplayed at the new scale. The displayed waveforms are called traces.

The processor performs the waveform arithmetic that generates the trace functions A+B, A-B, -A, -B, etc.; and the selected interpolation mode DOTS, LINEAR, or SINE. The data that results from these processing steps are called the trace buffers, and these are inputs to the processing steps which communicate to the hardware trace generator circuits, and to the calculation of voltages at the cursors.

The hardware trace generator circuits produce a digital output synchronized to the vertical scan rate of the CRT. This digital output is mixed with the outputs from the character generator and the graticule generator to form the pixel on/off signal sent to the CRT drive circuits on the CRT Driver board. The trace, character, and graticule generators are all controlled by the processor, and share the same dynamic RAM that the MPU uses. Regular access of dynamic RAM by the display generators satisfies the RAM refresh requirements.

Time Base Control

The Sweep and Record board contains the time base control circuitry. This consists of a 100-MHz crystal controlled oscillator; a programmable frequency divider the output frequency of which is switchable at the trigger event for dual time base recordings, and a trigger delay counter. The Time Base Control circuitry also generates the Convert Strobe signals which are sent simultaneously to both ADC boards.

When the trigger event occurs, the trigger delay counter counts upward at the sampling frequency, from the value preset by the processor prior to being armed. When a count of 999 is reached, this "top count" stops acquisition. No further Convert Strobe signals are sent to the ADC and the processor detects this by polling a port on the Sweep and Record board that indicates the acquisition is complete.

Triggering

There are five trigger sources available: channel A, channel B, external, line, and manual. The first three trigger sources are user input signals; and trigger level, slope, AC/DC coupling, and frequency dependent filtering are selectable for these. Trigger level, slope, AC/DC coupling, and filtering are not selectable for the last two trigger sources (line or manual). Channel A and channel B have their own trigger DACs (digital-to-analog converters) to supply a trigger voltage reference, and their own trigger slope, coupling and filtering selection circuits. These are located on the ADC boards except for the AC/DC coupling function which is on the Attenuator board. Channel A circuitry is used for external triggering except that the external trigger input has its own AC/DC coupling components.

The trigger output pulse from the channel A ADC board is sent to the channel B ADC board, which either passes it on to the Sweep and Record board, or blocks it and substitutes the channel B trigger output pulse if the channel B trigger source is selected.

Line trigger is a 60-Hz signal developed in the power supply and sent to the Sweep and Record board. Manual trigger is a signal developed by the MPU when the MPU writes to a port on the Sweep and Record board in response to the front panel MAN TRIG button being depressed.

The Sweep and Record board will not accept a trigger signal until after it is armed and a memory flush is complete. This ensures that no data in memory remains from a previous recording. Flush is only required and implemented when a recording is to contain pretrigger data.

The Sweep and Record board may also be programmed by the processor to implement auto-triggering. When enabled, auto-triggering causes a trigger to occur automatically if no other trigger event occurs within approximately 100 milliseconds after the completion of the flush.

Processor Operation

Control of the 4500 is performed by an 8088 microprocessor executing a program stored in 64k bytes of EPROM located on the CRT board. The 8088 is located on the MPU board along with 16k bytes of dynamic RAM, 256 bytes of nonvolatile CMOS RAM, interrupt arbitration circuitry, and the trace generation circuits.

On power up, or RESET from the CPU, the 8088 restarts at the beginning of its program. At this time the CPU reads the DIP switch on the MPU board to determine whether to operate in the user mode or one of the diagnostic modes.

On the MPU board, a 20-millisecond timer interrupt causes the processor to poll the front panel to determine if any key has been depressed. The MPU also uses the timer interrupt to decrement the count-down timers used to time the turning off of the floppy disk motor, and to schedule the automatic calibration of the ADCs. Other interrupts to the processor come from the Sweep and Record board when it is recording in roll mode, from the GPIB and RS-232C interface circuits when processor intervention is required, and from the floppy disk circuitry.

Auto Calibration

The processor performs periodic calibration of the ADCs. The processor computes settings to correct for gain and offset errors on the ADC board DACs. Gain calibration is done by using the offset DACs on the ADC boards as programmable DC sources. These generate test voltages that are routed into the input amplifier chain via reed relays. Using these voltages, the processor determines the thresholds that cause each ADC to generate its highest and lowest digital outputs. Then a DAC that controls the ADC gain is adjusted to bring the voltage difference that causes these highest and lowest outputs to the correct value.

Offset errors are corrected by grounding the attenuator input and adjusting a DAC that modifies offset.

The 4500 also has a user-initiated probe calibration feature. An ADC calibration is performed first, then a programmable DC source (channel B offset DAC) generates precision levels at the front panel CAL test point. The user is prompted to hook a probe, from either channel, to the test point and an approximation of the probes's attenuation identifies it as a x1, x10, or x100. A process similar to the ADC gain calibration process calculates the error introduced by the probe.

Peripheral Interfaces

An optional 5.25 inch disk drive attaches to the 4500. Control circuits on the Floppy Disk Interface board provide for storage and recall of digitized waveforms and instrument setup configurations. An I/O Interface Options board provides RS-232C, GPIB, analog averager, and DR-11B interfaces. The GPIB and RS-232C interfaces support remote control as well as remote access to acquired data. The rear panel analog plotter outputs are provided using circuitry located on the Sweep and Record board.

4500 DETAILED THEORY OF OPERATION

The 4500 Digital Oscilloscope is composed of the following boards and functional units:

MPU Board
CRT Driver PROMs
Sweep Record Board
ADC Board
Attenuator Board
Interface Board
Floppy Disk Option
Optional Floppy Interface Board
Keyboard
CRT Driver Board
Power Supply

Following paragraphs describe each board at the detailed level and include references to the schematics in Chapter 6.

MPU BOARD THEORY OF OPERATION
(Refer to schematic 0285-0046)

The following paragraphs describe the MPU Board at the detailed schematic level.

MPU Overview

The MPU board has an 8088 microprocessor, 16K of dynamic RAM, 256 bytes of CMOS RAM with battery backup power, control logic for seven processor interrupts, a 50-Hz timer interrupt oscillator, and data and address bus buffers. The MPU board also has the display generator, which generates the digital video and sync signals for the CRT driver on the CRT board. Logic on the MPU board is synchronized to timing signals derived from an on-board 40-MHz oscillator.

Micro Processor

The INTEL 8088 microprocessor U14D runs in MIN mode at a clock frequency of 4.44 MHz. The microprocessor executes a program stored in the EPROM located on the CRT board. Communication with this EPROM is via the motherboard.

16K Byte Dynamic RAM

Integrated circuits U19A/B through U22A/B are 16K X 1 bit dynamic RAMs. This RAM is accessed for read and write operations by the MPU and for read operations by the display generator. It is used by the MPU to store waveform data from the high speed acquisition memory, trace data (interpolated and otherwise processed waveform data), and other data required by system software. Data written into this RAM by the MPU is read by the display circuitry to generate video output. During system power up this RAM is tested and cleared to all zeros.

Refresh, RAS and CAS generation, and display/MPU access arbitration are discussed below.

256 Byte Non-volatile CMOS RAM

ICs U19F and U19G are 256 X 4 CMOS static RAMs. These provide 256 bytes of non-volatile storage and store system parameters so that the setup of the 4500 is not lost when power is removed. Battery BT1 maintains the 2 volts minimum necessary to retain data when primary power is off. Battery life is approximately 5 years.

****
* WARNING *
****

DO NOT ATTEMPT TO RECHARGE THIS BATTERY.
EXPLOSION AND BODILY INJURY COULD RESULT.

Transistors Q3 and Q4 turn off when the +5 supply drops, preventing the battery from supplying current to other devices on the board. Transistor Q2 ensures that the RAMs CS2* input (chip select) is held high by BT1 when the +5V supply is low, or when RESET is true. This ensures that memory contents will not be destroyed during power down and power up.

Processor/Bus Interface

When the microprocessor reads or writes data, it gates a 20-bit address onto pins 2 through 16, and 35 through 39. Latches U15E, U16E, and U17E latch this address using the signal ALE as a latch enable. The microprocessor then writes or reads data on 16 of these same pins via transceiver U14E. The transceiver is enabled by the DEN* signal from MPU pin 26. The transceiver direction (into the MPU for a read, or out of the MPU for a write) is controlled by the DT/R* signal from MPU pin 27. ICs U12D and U6C buffer the processor's RD*, WR*, and IO/M* signals.

I/O Interface

The 8088 microprocessor has two types of data transfers (reads and writes). These are memory data transfers and IO data transfers. When a memory transfer is performed, the IO/M* output (8088 pin 28) goes low. When an IO transfer is performed, the IO/M* output goes high. Integrated circuit U17C, a 512 X 4 bipolar PROM, decodes address lines A12 through A17 and the IO/M* signal. Using these inputs the PROM detects data transfers to the 16K dynamic RAM or CMOS RAM, or IO data transfers. The outputs of the PROM enable the dynamic or CMOS RAMs, or enable U16C (74LS138) which performs further decoding.

Integrated circuit U16C uses PROM output (U17C pin 9) and address lines A12 through A17 as inputs. U16C and the gates that follow it, decode the following signals:

Signal	Function
RD MPU*	Reads the DIP switch on the MPU board.
WRITE DISPLAY*	Lights the LEDs on the MPU board and writes to the display generator control latch.
WRITE INT MASK*	Writes data to the interrupt mask.
RD KBD*	Reads the front panel keys and resets the timer interrupt.

Memory and I/O Address Maps

The MPU transfers data to/from the various memories and IO devices by reading/writing to addresses associated with these devices. Most of the address decoding is done on the individual boards containing these devices. The hexadecimal address or address range of each device is listed below:

Memory Address Range	Device
00000 - 03FFF	Dynamic RAM
04000 - 040FF	CMOS RAM
06000 - 063FF	1K RAM on disk option board
F0000 - FFFFF	64K EPROM memory on CRT board

IO Address Range	Device
00 (Write)	Interrupt mask latch on MPU
00 (Read)	Read 8 bit DIP switch on MPU
10 (Write)	LEDs and display generator control latch on MPU
20 - 2E (Read)	Scan keyboard on front panel
2F (Read)	Actuate clicker on front panel
30 - 36 (Write)	Latches on channel A ADC
40 - 46 (Write)	Latches on channel B ADC
50 - 5F (R/W)	Latches, strobes, and outputs of Sweep and Record board
60 - 6F (R/W)	Latches and outputs of floppy disk interface
70 - 7F (R/W)	Latches, strobes and outputs of Interface Options board

Jumper connections E4-E5 (link to disable CMOS RAM) and E6-E7 (link to disable floppy disk RAM) should not be connected. These pull inputs of the decoder PROM, U17C to ground; and allow the use of 64K dynamic RAMs during prototype development.

Interrupt Control

There are six possible sources of a processor interrupt. The signals that represent these interrupts are decoded by the 74LS148 priority encoder, U11E. If any interrupt signal goes low; the GS output of U11E (pin 10) goes low; and the logic levels on the A0, A1, and A2 outputs of U11E (pins 9, 7, and 6) will indicate which interrupt signal went low. If more than one interrupt signal goes low at the same time; the A0, A1, and A2 outputs will represent the highest priority interrupt.

When the GS output of U11E goes low, it activates the output of a 74LS151, U12E. Data selector, U12E selects one of eight signals to be transferred to its output. The signal selected is determined by the A0, A1, and A2 outputs of the priority encoder U11E. If the signal selected is a high, a high will be sent to the INTR (interrupt) input of the processor. A high will only be sent; and the processor will only be interrupted; if the output of the 74LS273 flip-flop, U13E has been set high. The processor loads U13E to enable, or to mask out, the various interrupt sources.

The six interrupt sources, in order of decreasing priority, are as follows:

Signal Name	Signal Source
IRQ6	Floppy Disk Controller
IRQ5	GPIB Controller
IRQ4, IRQ3	RS-232 Controller
IRQ1	Sweep and Record
11E pin 10	50-Hz Timer

When the microprocessor receives an interrupt, it responds with an interrupt acknowledge signal by pulling low its INTA* line, pin 24. The INTA* signal going low clocks flip-flops U8D; and gates the A0, A1, and A2 outputs of U11E onto the microprocessor data bus. This allows the MPU to determine which source generated the interrupt. When the MPU responds to the interrupt it writes the interrupt mask again, and thereby resets flip-flops U8D.

50-HZ Timer

The 50-Hz timer uses an NE555, U8F as an oscillator. When the output of the NE555 (pin 3) goes high, it causes the Q* output of flip-flop U9D (pin 8) to go low. This output is an interrupt source. When the processor responds to this interrupt, it scans the keyboard to check for pushed keys, and it decrements software timers used in auto calibration and in disk operations. Scanning the keyboard generates the RD KBD* signal. This signal causes the keyboard to be read and also resets flip-flop U9D.

Display Generator Overview

The display generator consists of a trace generator, a character generator, and a graticule generator. Each generator receives data from the dynamic RAM, to produce a digital video output synchronized to the vertical and horizontal scan rates of the CRT. The processor can disable the outputs of any of these generators. Three video outputs are combined and gated with a video blanking signal during retrace. This occurs in flip-flops U6B.

The CRT raster consists 500 vertical scanlines displayed on the screen. There are 512 pixels per vertical scanline.

Trace Generator

Data for generating traces is written to dynamic RAM by the MPU, and is read by the trace generator hardware. Four bytes are written for each scanline. During a scanline, the trace generator reads the four bytes. The scanline is divided into four quarters. In each quarter, the byte that corresponds to that quarter determines where a dot will be drawn if Dots mode is active, or where the drawing of a vertical line segment will begin or end if dot joining is active.

As each byte is read from dynamic RAM it is clocked into flip-flop U3F. After it is clocked into U3F it is also clocked into a four word register file consisting of U3E and U4E. At the beginning of each scanline quarter, the outputs of flip-flop U3F are loaded into counters U3C and U4C, and the outputs of register file U3E/4E are loaded into counters U3D and U4D. The register file outputs however, correspond to data from the previous scanline. That is, the register file delays the bytes passing through it by one scanline time.

During the time a scanline quarter is being scanned, counters U3C/4C and U3D/4D count up. When the first counter reaches its top count, the J and K inputs of flip-flop U4A (pins 3 and 2) go high, and the next clock, toggles the flip-flop. This causes the scanline to become illuminated by toggling the output of the other half of flip-flop U4A, pin 7. When the other counters (U3C/U4C or U3D/4D) reaches their top count, the output of flip-flop U4A, pin 6, toggles again turning the scanline off. This toggling on and off assumes that dot joining is active. If dot joining is not active; the reset input of U4A, pin 15 will be low and this flip-flop will not toggle.

If dot joining is not active the following occurs: As a scanline quarter is being scanned, when counter U3C/U4C reaches its top count, the output of flip-flop U4A (pin 7) turns on for one pixel time. This produces a dot on the scanline. This flip-flop also produces a one pixel dot, if dot joining is active and if both counters reach top count simultaneously. This is necessary; because the output of U4A, pin 6 will not toggle in this case.

Character Generator

The character generator can display 25 rows and 62 columns of characters, from a 128 character set. Rows are 20 pixels high and columns are 8 pixels wide. Characters are 16 pixels high and 8 pixels wide. There is a 4 pixel gap between characters vertically and no gap horizontally.

Each character position on the CRT has a corresponding address in the dynamic RAM. At this address, a one-byte code defining the character to be displayed is written by the MPU. The character defining codes are fetched by the character generator, synchronous with the scanning of the CRT, and latched into flip-flop U4F. IC U5F is a 2K X 8 EPROM. For inputs this PROM uses the character code; signals L0, L1, and L2; and the output of flip-flop U7E, pin 9. Outputs L0, L1, and L2 of the scanline counter signify which of eight columns within a character the current scanline corresponds to. The output of flip-flop U7E indicates whether the scanline is currently at the top half or bottom half of a character position. The PROM then outputs eight bits which represent the desired dot pattern that defines the top or bottom half of one of the eight columns of the desired character.

The PROM output is parallel loaded into a 74LS299 shift register, U6F. This bit pattern is shifted out serially to produce the character video data.

The most significant bit of each character code in RAM is high for a blank character, and low for a nonblank character. If a character is nonblank; this low logic state causes the Q output of flip-flop U7F, pin 9 to go low. This inhibits the display of graticule and trace pixels. The purpose of this is to prevent the display of trace and graticule pixels from obscuring the characters.

Graticule Generator

Before the display of each scanline begins, a 74LS399, U5E stores 4 bits of data from the dynamic RAM. These bits represent which of sixteen possible graticule patterns to draw on the scanline. These bits are inputs to a 1K X 8 PROM, U2F. The PROM also receives signals T3 through T8 as inputs via flip-flop U2E. The T3 through T8 bits represent the current position of the scanline on the CRT as it is being drawn. The PROM parallel loads the pixel information representing the graticule pattern, into shift register U1F. The shift register outputs the pixel information serially to produce the graticule video data.

Oscillator and Clock Generation

The clock oscillator consists of transistor Q1, crystal Y1, and associated circuitry. It oscillates at 40 MHz and is divided by U2B, to produce two 20-MHz clocks that are the inverse of each other, and two 10-MHz clocks that are the inverse of each other. The 40-MHz signal is also divided by 3 in a 74S112, U7D; and passed to the 8284 clock generator, U11D. The 8284 produces the 4.44-MHz processor clock with a 1/3 duty cycle. The 10 MHz is separated into five phases of 2 MHz by a 74LS112, U12C; and by a 74LS195 shift register, U14C. The five phases are signals K0, K1, K2, K3, and K4. These are used by U13B and U14B to generate the RAS*, CAS*, WRITE*, and R*/C signals that control the dynamic RAMs.

Display Timing

Counter U1D and U2D generate signals T1 through T8 which count vertical position, from 0 to 255, during each scanline. Top count from this counter, (U1D pin 15) causes vertical blanking to be generated (U8C pin 6) which then causes vertical sync to be generated (U8C pin 9); and also increments the counter that counts which scanline is currently being drawn (U8B, U17B, and U18B). This scanline counter counts from 12 to 511, generating signals L0 through L8. Top count from this counter (U18B pin 15) generates horizontal blanking (U9C pin 6), and horizontal sync (U10D pin 4).

A 74LS161 counter, U11C, counts starting at the bottom of each scanline to generate the signal GRAT LATCH. This signal is used to latch dynamic RAM data into the graticule generator.

CRT BOARD, EPROM MEMORY
(Refer to schematic 0285-0051, sheets 2 and 3)

The following paragraphs describe the CRT board at the detailed level.

Overview

The CRT board includes the EPROM memory which contains the microprocessor software. The board operates with either sixteen 2732 (4K X 8) EPROMs or eight 2764 (8K X 8) EPROMs. Sixteen sockets are provided; eight 28 pin, and eight 24 pin. When 2732 EPROMs are used, those eight which go into 28-pin sockets are loaded with socket pins 1, 2, 27, and 28 left unfilled. Jumper pads E1-E2 are connected to enable operation with 2764s, but are left open for 2732s.

CRT EPROM Operation

The MPU board generates addresses A0 through A19, and the read signal RD*. These are buffered by U37, U38, and U39 on the CRT board. The EPROM is addressed when A16 and A17 are high and RD* is low. This decoding is done by AND U19 and U42 (2 NAND gates). The decoder generates an onboard RD* signal at U42 pin 6. The onboard RD* signal latches the address into U38 and U39, pulls low the output enable lines of the sixteen EPROM devices U21 through U36, and enables the data bus driver U13.

Latched address lines A12 through A15 are decoded in the two 74LS138 decoders U40 and U41. One of the output lines, from these two decoders, selects the EPROM to be read by pulling its chip enable line low.

SWEEP AND RECORD BOARD THEORY OF OPERATION
(Schematic 0285-0261)

The Sweep and Record board consists of six subsystems as follows:

1. Memories (A and B)
2. Memory timing generators
3. Record control
4. Sample rate counters
5. MPU interface
6. Plotter interface

Each subsystem is described in detail in following paragraphs.

Memories (A and B)

There are two memories with a capacity of 1000 samples each. In dual channel mode one memory records data from channel A and the other records data from channel B. In single channel mode the data from the active channel is routed to both memories, permitting a recording length of 2000 samples.

Each memory is divided into two banks. Each bank is divided into two phases. In dual channel mode, successive samples from channel A are placed in alternate phases of one bank of channel A memory until the bank is filled, then successive samples are placed in alternate phases of the other bank of channel A memory until filled. Samples from channel B are stored in the channel B memory in the same manner.

In single channel mode, the samples from the active channel first fill one memory as described above (in alternate phases of one bank, then in alternate phases of the second bank), then fill the other memory as described above. Two phases are used so that samples taken every 10 nanoseconds can be recorded in ICs with access times slower than 10 nanoseconds.

Differential ECL data from the ADC boards, is transferred via the mother board, and is received on the Sweep and Record board by the 10115's at U2F, U3F, U4F, and U5F (see schematic page 1). The outputs of the line receivers are applied to both the A and the B memory systems. The A system will be described here. The B system is identical.

Channel A Memory

The memory has two sets of input latches or "pre-memories" which are clocked alternately by the signals LAA1 and LAA2. LAA1 and LAA2 are derived from the DATA READY strobe which comes from the ADC (see schematic page 6). This two phased system allows the use of RAMs whose write cycle is longer than the fastest sample interval of the instrument (10 nanoseconds).

Notice that each phase of the system has two sets of pre-memories whose outputs are wire ORed. When in dual channel mode, or in single channel mode with A only selected; ICs U3C, U3D, U5C, and U5D (see schematic page 1) are disabled by the signal AA, and channel A data is applied to the memories via U2C, U2D, U4C, and U4D. In single channel mode with B only selected; ICs U2C, U2D, U4C, and U4D are disabled by AA*, and channel B data is applied to the A memory.

Each phase of the memory contains two banks of two 10422, 256x4 ECL static RAMs. Each time the address counter completes 250 counts, the 10141 at U1B reverses the state of the bank select inputs to the RAM's. The next 250 samples are then written to the other bank of RAM's.

In dual channel mode, the two banks in each memory are alternately enabled, causing the memory to wrap around at the end of 1000 samples. In single channel mode, after 1000 samples, both banks of the A memory are disabled while the data is being recorded in the B memory. The B memory is disabled while writing to the A memory.

Addresses for phase 1 are provided by the two 10016 counters at U1A and U2A, and the bank select bits for phase 1 are provided by the 10141 shift register at 1B. The outputs of the counters and the shift register are latched in the 10186 ICs at U1C and U1D. The outputs of these latches are used to address and bank select phase 2. Notice that the low order counter (U2A) is preset to 0110 when the entire counter reaches its top count. This causes each bank of each phase to be 250 samples long instead of 256, for a total memory length of 1000 samples per channel.

The outputs of each bank of RAM are wire ORed. The block select signal determines which set of outputs will be active when the RAM is read from, just as it selects the active bank when the RAM is written to.

The outputs of each phase of the A memory are multiplexed with the outputs of the same phase of the B memory. Multiplexing takes place in U6F, U7F, U8F, and U9F (see schematic sheet 6). Signals controlled by the microprocessor are used as the select inputs of the multiplexers. These select the data to be read by the MPU. The data to be read is shifted to TTL by U10F and U11F. The data is gated onto the MPU bus by the LS244 at U12F, or sent out connector J2 pins 35-42 to the DMA circuitry on the Interface Options board.

Memory Timing Generators

The DATA READY signal is transmitted from each ADC to the Sweep and Record board with each new sample. These strobes are received differentially in the 10115 line receiver at U1E (see schematic sheet 6). Channel A operation will be discussed here. Channel B operation is identical.

The DATA READY signal is divided into two control strobes, (LAA1 and LAA2) which are half the frequency of the DATA READY strobe, and are 180 degrees out of phase with each other. These signals drive the two phases of the memory system. When in dual channel mode, or in single channel with A only selected, this division is accomplished in the 10231 at U6D. When single channel B only mode is selected, U6D is held reset by the signal AA*, and the channel A control signals are driven by the channel B strobe via the 10231 at U6E. The outputs of U6E are wire ORed with the outputs of U6D.

The leading edges of LAA1 and LAA2 latch new data into the pre-memories, advance the RAM address for the appropriate phase, and fire a chain of one shots (U7D, and U7E) which generate the write enable signals for the RAMs.

Two one-shots are required to generate each write enable signal at the proper time. To use phase 1 of channel A as and example, the leading edge of LAA1 clocks one half of the 10231 at U7D. The output of U7D at pin 2 is a negative going pulse whose width is controlled by R112 and C46. The trailing edge of this pulse clocks the other half of U7D whose output at pin 15 is the write enable signal for the RAMs. R72 and C47 control the pulse width of the write enable signal. This arrangement allows precise control of the position of the write enable signal relative to the change in the data and address.

When the microprocessor is ready to read the data that has been recorded it sets READ MODE true. This causes the write enable flip-flops to be held in a set state.

Record Control

The Record Control circuits consist of the trigger selection and synchronization flip-flops; and the trigger delay counters, which position the end of the recording relative to the trigger.

The output at pin 2 of the 10231 flip-flop at U16A (see schematic sheet 3) must be set to enable the start of an acquisition. This is accomplished by either an MPU control pulse, or by being clocked by an EXTERNAL ARM signal. The other half of U16A, which is controlled by the MPU, disables the external arm function. After U16A pin 2 is set, trigger acceptance is held off by flip-flop 15A until a full rotation of the memory address counter is detected by pin 6 of flip-flop U17B. This guarantees that memory contains valid data, even if a trigger is received immediately and the trigger delay is short.

When U15A pin 3 goes low (see schematic sheet 3), the clock inputs of U14A are enabled. The D inputs of the flip-flops in U14A are the trigger source selection signals from the MPU, which are clocked through by the trigger pulses coming out of U18C pin 14. The outputs of U14A, are wire ORed with the output of the auto trigger timer made up of U17A, U20A and U19A. The signal at this node is called ACQUIRE. ACQUIRE is synchronized to the sample clock in the 10231 at U13A, and the complement output of this flip-flop (ACQUIRE*) is used to control the sample rate switching and the delay counter.

There are two modes of operation for the circuit after ACQUIRE* goes true. If the user has selected any amount of pretrigger recording, the MPU control bit PRE*/POST is set low. This, along with ACQUIRE* going low causes the output of the 10102 at U16B pin 14 (see schematic sheet 3) to go high. This makes the signals SPEED and SPEED* (U18B pins 2 and 3) change state, changing the sample rate to the one selected for post trigger recording. Sample rate switching will be discussed in detail in the Sample Rate Generation section below. ACQUIRE* also enables the trigger delay counter (U16C, U17D, and U16D) which was preset by the MPU to the complement of the number of samples of delay required. The roll over of the trigger delay counter clocks the 10231 at U18B pin 9, causing signal EOA to go true. EOA is ORed with the rear panel EXTERNAL CLOCK GATE signal (see schematic sheet 5), and is applied to the input of flip-flop U20F. When the next sample is recorded, EOA gated with EXTERNAL CLOCK GATE is clocked through the 10231 at U20F. The output of U20F at pin 2 is signal EOADEL which gates the ADC strobes off, terminating the recording.

If no pretrigger recording is needed, PRE*/POST is set high by the MPU. This prevents ACQUIRE* from changing the state of SPEED and SPEED*, and thereby prevents sample rate switching at this time. The delay counter is enabled however. The counter counts up to its top count at the pretrigger sample rate, from a preset count calculated by the MPU. When top count is reached, the rising edge of the TC* signal at U16C pin 4, (see schematic page 3), clocks the flip-flop at U18B, causing SPEED and SPEED* to change state. This switches the time base circuits to the post trigger sample rate. The delay counter counts at the post trigger sample rate for 1000 counts, at which time the next rising edge of TC* again clocks U18B and causes EOA to go true. This begins the end of record sequence as described above. The use of a dual counting rate, with the pretrigger rate being slow, allows for trigger delay times much longer then would be possible with the same counter operated at the post trigger rate only.

The clock for the delay counter (SAMPLE 1) is gated through the 10102 at U16B (see schematic sheet 5) by the output of a 10231, U13A pin 3. When single channel mode is selected, U13A divides the sample rate by two, causing SAMPLE 1 to be half the sample rate. This allows the double length memory associated with single channel recordings to be completely filled with data at the post trigger sample rate, even though the counter is only 1000 counts long.

When operating in Roll Mode, the signals BYTE MODE and ROLL MODE are set true by the MPU. This disables the delay counter. Roll Mode recordings are terminated under MPU control.

BYTE MODE places a high on U20F pin 10 (see schematic sheet 3), the D input of a 10231 flip-flop. The signal SAMPLE 2 clocks U20F pin 11, generating an interrupt request to the MPU. The MPU then reads the new data. Reading the ADC data resets U20F until the next sample is recorded.

Signals ARMED, ARM DEL (indicates a flushed condition), ACQUIRE, and EOA are available for record control status monitoring by the MPU. This is via the 10104 at U15B (see schematic sheet 3). MPU control signal "READ 1" enables this information onto the ECL data bus where it is wire ORed with the outputs of the high speed RAM data multiplexers.

Sample Rate Generation

All internal sample intervals are derived from the 100-MHz oscillator which consists of Q2, Y1 and associated parts (see schematic sheet 5). Variable capacitor C102 permits fine adjustment of the oscillator frequency.

An external clock source can be substituted for the internal oscillator under MPU control. This selection takes place in the 10111 at U19F.

The 100-MHz signal from the oscillator is applied to the clock input of the 10016 synchronous binary counter at U19E. The top count output of U19E is applied as the clock of a chain of decade ripple counters (U19D, U19B, U20B, U20C, U21C, and U20D) and to one of the data inputs of the 10164 data selector at U20E. The other inputs to U20E are the outputs of the decade counter chain.

Control bits from the MPU for the programmable counter and the data selector are stored in the 10153 quad latches at U18E, U18D, U21E and U21D. These latches have gated outputs which are wire OR'ed in pairs. The gating signals are SPEED and SPEED*. When these signals change state, as described above, new control information is presented to the counter and data selector causing the sample rate to change to the post trigger rate.

The selected sample rate is gated with EOADEL in the 10H102 at U18F. The outputs of U18F, pins 9 and 15, are the ADC strobe which is routed to the ADC boards differentially via the mother board.

An external CLOCK GATE signal is the applied to U20F pin 7, a 10231. Pin 6 of U20F is clocked by the sample clock. When CLOCK GATE goes high, pin 2 of 20F is caused to go high by the sample clock. Pin 2 is wire ORed with EOADEL which gates off the signals SAMPLE 1 and SAMPLE 2. This inhibits any more samples from being recorded until CLOCK GATE goes low and is again clocked through U20F.

When the microprocessor reads the memory, both internal and external clocks are disabled. Each read of the high speed memory generates an R SAMPLE pulse (see schematic sheet 3) which strobes the ADCs and is returned to the memory system as DATA READY strobes. This increments the memory addresses.

MPU Interface

Three 74LS138 ICs at U13D, U14D, and U14C (see schematic sheet 4) decode the MPU address bus; and RD*, and WR* signals. The outputs of these decoders are used in two ways. Some act as latch enables to write the contents of the data bus into holding registers such as the 10153s which hold the sample rate control data. Others act directly on the Sweep and Record circuits by generating signals such as MANUAL ARM, MANUAL TRIGGER, and FE RESET.

Octal latches U14F and U15F hold the static mode control bits.

All TTL signals which must interface with ECL circuits are level translated in 10124 level translators.

The ECL data bus which carries the Record Control status and the output data from the high speed RAM is translated to TTL levels in the 10125s at U10F and 11F (see schematic sheet 6). The outputs of the translators drive the circuits on the Interface Options Board via the mother board, and the inputs to the 74LS244 buffer which drives the MPU data bus.

Plotter Interface

The PLOTTER X and PLOTTER Y output functions are provided by two NE5018 8-bit DACs at U16F and U17F (see schematic sheet 4). The NE5018 has its own internal latches for digital data from the MPU. Address decoding is provided by the MPU interface circuitry to load the data into the internal latches. This address decoding circuitry also allows storing the PEN LIFT signal into the 74LS273 static control register at U14F.

ADC BOARD THEORY OF OPERATION
(Refer to schematic 0285-0056)

The following paragraphs present the theory of operation for the ADC Board at the detailed schematic level.

ADC Board Overview

The CHA and CHB boards are identical except that link W8 is cut for address decoding of CHA, link W9 is cut for decoding CHB, and the components for the external trigger function are only on the CHA board. The links are shown near U59 on sheet 13 of the schematics.

The ADC board contains the following:

- A programmable attenuator and two amplifiers to present the analog input signal to the track and hold,
- A track and hold and its associated pulse generator,
- A track and hold to ADC buffer amplifier,
- Eight folding amplifiers, an analog combiner, and a digital decoder for the first part of the ADC,
- A four-bit flash converter and associated latch for the second part of the ADC,
- A pulse generator to drive the latches and track and hold,
- LED drivers that indicate if the input signal is inside or outside full scale range,
- A set of reference voltage sources for the ADC and offset generators,
- Trigger source selector, adjustable trigger level reference voltage source and trigger comparator,
- Adjustable voltage sources for input offset, offset correction, and gain correction circuitry,
- Microprocessor interface,
- Power supply regulation.

Programmable Attenuator
(Refer to schematic sheet 1)

The signal from the Attenuator board is applied via coaxial cable to J2, and then to RP1, which with relays K1, K2, and K3, forms a programmable 1, 2, 5 attenuator. The full scale sensitivity of the 4500 is adjusted by the settings of this attenuator and the 1M ohm Input Attenuator on the Attenuator board. The gain from the front panel input BNC to J2, with the input attenuator set to X1, is approximately X2. The output from the relays is fed to Q1, pin 2, which is part of the first amplifier. The full scale sensitivity at this point is 160 millivolts.

First Amplifier
(Refer to schematic sheet 1)

Op amp Q1, transistor array U2, Q5, Q6, Q2, and Q4; form a non-inverting feedback amplifier with a gain of approximately 5.86. The dual matched FET Q1, and the differential pair in U2, amplify the difference voltage between the input and the feedback from the output via R29, and R15. The amplified error voltage across R18 drives the output via emitter followers Q2, and Q4. Source currents for Q1 are provided by the transistors in array U1. Current for the differential pair in U2 is adjusted by potentiometer R12. The Op Amp in U3 connected to R12, monitors the difference between the voltage on R9 and the voltage on the wiper of R12, and via R7 and the emitter follower in U2 reduces this to voltage to zero.

A similar arrangement enables the voltage at the top of collector load R20 to be set by R34, an op amp, and emitter follower Q5. The voltage at top of collector load R18 is set by R21, an op amp, and emitter follower Q6. The overall gain of 5.86 is set by R25.

With zero input voltage, the required output voltage of 3.96 volts is set by current source Q3 to approximately 4 milliamps. This is accomplished by adjusting potentiometer R35.

The internal trigger pickoff is provided by the attenuator comprised of R48, R663, and R56. The 3.96 volt offset at the output of the first amplifier is removed from the trigger path by the voltage drop generated by current source Q7 across R48. This is adjusted to approximately 7.7 milliamps by R30, to bring the voltage at the top of R663 to zero. Gain of the internal trigger channel is adjusted by R663.

Second Amplifier
(Refer to schematic sheet 2)

Transistor arrays U5, and U6; and transistors Q8, and Q11; form a shunt feedback amplifier whose gain is set to 1.6 by feedback resistor R95 and input resistor R94. The junction of R94 and R95 is a virtual ground point. The difference in voltage between the output of op amp U4, pin 7, and the virtual ground is amplified by the differential amplifier connection of transistor arrays U5, and U6.

The amplified error signal at collector load R87, is applied via emitter followers Q8, and Q11 to one of the output load resistors, R106. A balance of currents is set up at the virtual ground such that the input current in R94, which is approximately 11 milliamps, plus the current in R95, is equal to the current set up in current source Q10. With the virtual ground at -7 volts, and an output voltage at the top of R106 of -4.5 V, Q10 current will be approximately 12.4 milliamps. This is adjusted by R76.

Op amp U4 (pins 12, 13, and 14) monitors the voltage difference between source of Q10 and the wiper of potentiometer R76. Feedback via R90 reduces this difference to zero. Similarly, Op Amp U4 (pins 1, 2, and 3) sets the current in transistor array U6, by R59. The virtual ground voltage is set by Op Amp U4 (pins 5, 6, and 7) which is connected as a shunt feedback amplifier whose input is the +10 volt reference. The ratio of R63 to R62, together with the feedback action, produces 0 volts on pin 6, and -7 volts on pin 7. The voltage at the bottom of load R106 is set by a similar circuit using op amp U4 (pins 8, 9, and 10) and R82, and R80 as feedback resistors. The output at U4 pin 8 is buffered by emitter follower Q9.

The voltage difference across R106 is set by R80 to approximately 1.2 volts, to set about 50 milliamps in R106, output transistor Q11, and R117. Resistor R117 in the collector of Q11 is equal to R106 so that the signals at the emitter and collector of Q11 are equal in amplitude and out of phase. The collector output provides the signal to be sampled by the track and hold bridge, while the emitter signal and the collector signal buffered by emitter follower Q78 are also used by the track and hold circuit.

Track and Hold
(Refer to schematic sheet 4)

The diode bridge CR9 can be in one of two states, heavily conducting with current supplied by T1, or reverse biased by a voltage supplied by T1. In the conducting state the bridge presents a low impedance between the signal input and hold capacitor C70, of about 10 ohms, so that the voltage on C70 tracks the signal voltage.

In the reverse biased state, the bridge is a high impedance. Residual capacitive feed through is balanced out by the injection of an antiphase signal via R715, and C67. Fast current switch Q13, Q76, Q15,and Q77; turns diode bridge CR9 on and off. An 80-milliamp current source, made up of Q16 and U7 (pins 12, 13, 14); provides current to differential pair Q15/Q77. A balanced ECL signal is applied through T3 to amplifier Q17/Q78; whose output is connected by T2 to Q15/Q77; so that the 80 milliamp current can be diverted through either Q15 or Q77. If the base of Q15 is positive with respect to the base of Q77; current flows through Q15, and Q13; and splits about equally through path T1, CR9, T1, R129, R130 and path R131, R132. The forward voltage drop across CR9 reduces the bridge current to about 34 milliamps.

A current sink of approximately 100 milliamps, Q12; provides current to emitter follower Q78 (schematic sheet 2), and also balances the 80 milliamps through Q13 such that no current flows out of the bridge into the signal source. The currents and voltage drops in the four arms of the bridge are then equal; and the junction of R129, R130, R131, R132 is about +2.4 volts relative to the signal input. If the base of Q15 becomes negative with respect to the base of Q77, the 80 milliamp current is diverted into Q77/Q76. No current flows in the bridge or R131/R132 and 80 milliamps flows in R129/R130. The voltage at the junction of R129, R130, R131, and R132 is unchanged so that a reverse bias of 4.8 volts centered about the signal voltage is applied to the bridge via T1.

The bootstrap emitter follower, Q78 (schematic sheet 2); and T1 reduce loading effects on the signal path; and T1 further balances the drive to CR9. Current source Q12 is set with R104 acting through U7 (pins 8, 9, 10). In normal operation the system works in the track mode until a sample is requested by a pulse from the Sweep and Record board. The hold mode is then entered for a period of 7 nanoseconds. At the maximum rate (100 MHz) the time in track mode is reduced to 3 nanoseconds.

Track and Hold Buffer Amplifier
(Refer to schematic sheet 3)

The sampled signal voltage on C70 (schematic sheet 4) is applied to the high input impedance of the third stage feedback amplifier. This amplifier has a non inverting gain of approximately 2.64. The circuit is similar to the 1st amplifier with Q14, a dual FET, and a differential pair in U8 forming a differential amplifier whose input is the error between the voltage on C70 and the attenuated output voltage returned via potential divider R411/R408. The amplified error voltage at collector load R397 drives the output through emitter followers Q43 and Q44.

Current sources for the dual FET are provided by transistors in U9. Current in U8 is set up by R427 and op amp U32 (pins 12, 13, 14). Similarly, the voltage at the top of collector load R118 is set by R422 and Op Amp U32 (pins 5, 6, 7); and the voltage at top of collector load R397 is set by R404 and op amp U31 (pins 8, 9, 10).

Quiescent voltage at the output (the junction of R412 and R411) is required to be zero for an input quiescent voltage of -1.2 volts. A current source applied through R407 into the feedback network achieves this, and is adjustable by R424. Current in the output transistor Q44 is set by Op Amp U31 (pins 12, 13, 14) and Q45.

The feedback from pin 14 via Q45 and Q44 makes the voltage on pin 12 equal to that on pin 13. This makes the current in Q44 independent of output voltage for normal operation and adjustable with R414. The voltage drop across R412 of approximately 2.3 volts provides enough collector voltage for the differential pair in U8. Gain is adjusted by R409, a shunt across R408. Pulse response is set by networks C202, C201, R681; C200, R714; and also feedforward via R722, emitter follower in U8, C407, and R721.

Analog to Digital Converter
(See Figures 5-2 and 5-3.)

The ADC consists of two basic parts:

1. A set of eight folding amplifiers which produce the first four most significant bits, and an analog residue.

2. A four-bit flash converter to produce the four least significant bits.

The operation of the folding amplifier array will be explained with the aid of the simplified schematic (Figure 5-2) and idealized waveforms in Figure 5-3.

Only amplifiers A and B of array A through H are shown in Figure 5-2. The full scale range is set by the reference chain running between +2 and -2 volts, to be 4 volts total. The difference between Ref A and Ref B is 1/8 full scale or 0.5 volts. This gives a sensitivity at the ADC input of 15.7 millivolts for the least significant bit (LSB).

For correct operation Ref A is placed 16 LSBs below the +2 volt reference. If the input signal is more negative than Ref A; the output from amplifier Q1A/Q2A is saturated; with Q2A taking all the current provided by R5, and transistor Q1A being cut off. This output drives PNP comparator pair Q3A/Q4A, called Comp A, to generate a zero logic level.

As the input voltage increases, positive voltage VA moves from point X in Figure 5-3, more positive, to a maximum (occurring when Vin=Ref A), then negative back down to level X. This occurs because the voltage at the emitters of pair Q3A/Q4A, due to the diode action of their base-emitter junctions, will equal the most negative collector voltage of Q1A/Q2A plus one base-emitter bias voltage. This bias voltage will be relatively constant as the current is switched from Q4A to Q3A, being compressed by only about 20 millivolts at the fold point.

Amplifier Q1A/Q2A is set by the ratio of R1 to R3, to have a gain of four from the input to either R1 or R2, so VA must change by 63 millivolts to change the final digital output by one LSB. The rounding of the response at the fold point causes less than one half LSB of error. For inputs more positive than Ref A, the Comp A output will be a logic one.

Folding amplifier B works in the same way, producing a digital output labelled Comp B Output, and an analog output labelled VB. The analog outputs from all the comparators are combined by the action of Q5A, Q5B, Q5C, ... Q5H; to give the final folded output called the Analog Residue. This will be the most positive signal of the group VA . . . VH. The negative fold points are similarly rounded by about 20 millivolts.

The positive fold points occur at the switching points of Comp A, Comp B, etc. For correct decoding of the folding amplifier array output into four-bits, fifteen comparators are required. The seven comparators between stages (Comp AB, COMP BC, . . . COMP GH) have their outputs aligned with the negative fold points. For the A and B sections this is done by Q5A/Q6A, which compare the inphase output of Q1A/Q2A to the antiphase output of Q1B/Q2B. The biasing of this comparator (COMP AB) makes its output change at point Y in Figure 5-3.

Similarly, comparators BC, CD, . . . GH give digital outputs at the other negative fold points. The fifteen comparator outputs are latched before being encoded into a four-bit Gray code, and sent to the Sweep and Record board. The analog residue signal is applied to a four-bit flash converter, the outputs of which are similarly latched before being sent to the Sweep and Record board.

Detailed Description of Folding Amplifier
(Schematic sheets 6, 7, and 8)

Sheet 6 of the schematic shows the two most positive folding amplifiers of the array, eight emitter followers that generate the final folded output, and the second-rank four-bit flash converter. Sheets 7 and 8 show the other six folding amplifiers.

Comparator #1 (schematic sheet 6), corresponds to folding amplifier A, comparator #3 corresponds to folding amplifier B, and Comparator #2 corresponds to Comp AB in the Simplified Folding Amplifier Array, Figure 2. The signal and reference inputs to all the folding stages are buffered by emitter followers. For the comparator #1 stage, these are two transistors in array U34.

The signals then pass via T11 and provide HF balance to a differential amplifier consisting of transistor array U71. This has emitter follower outputs driving the folding PNP pair Q75/Q74. The folded signal routed from the common emitter point; through R629 and L20; to Q57, an NPN emitter follower. The other folding amplifiers drive similar NPN transistors.

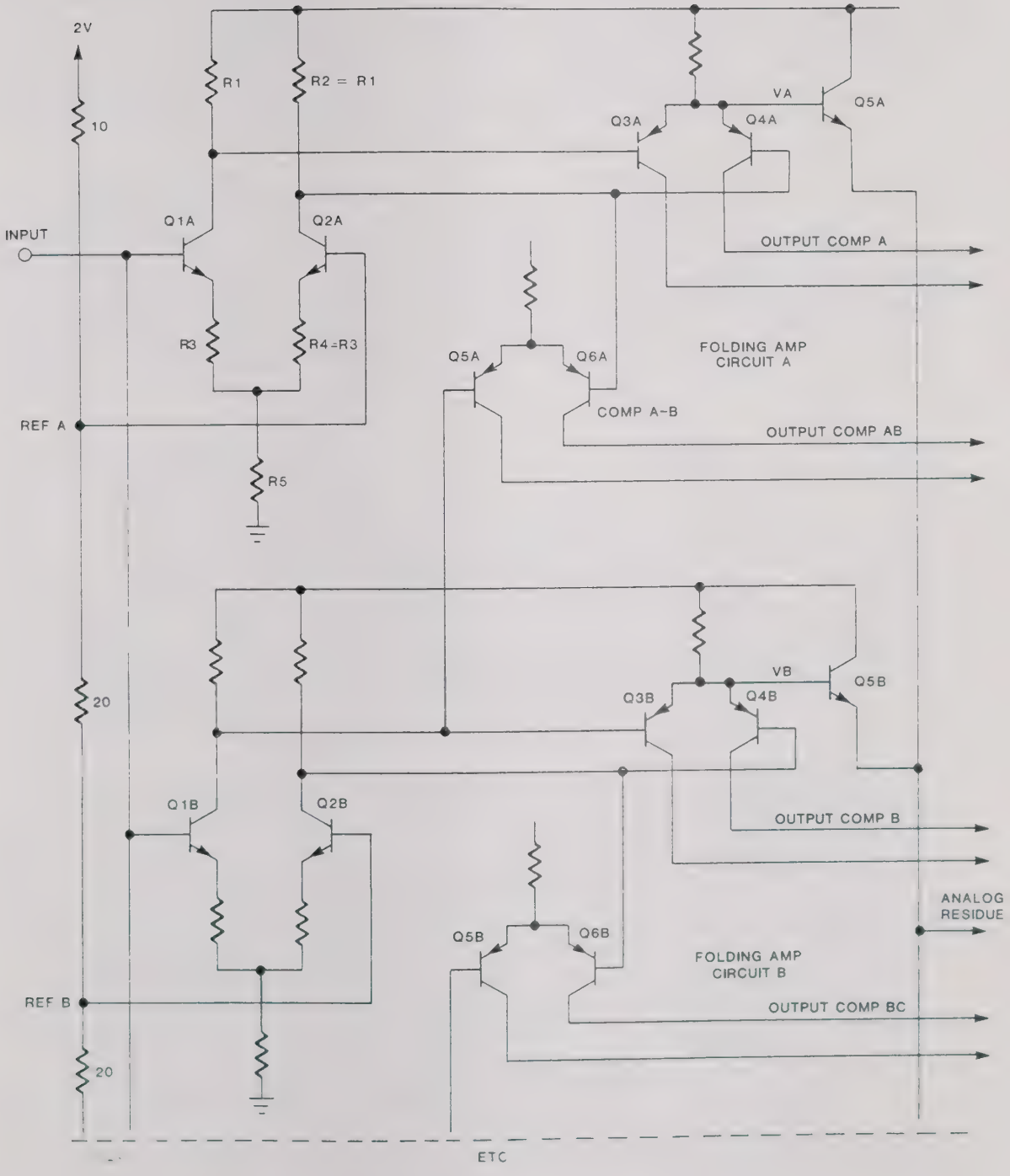


Figure 5-2. Folding Amplifier Array Simplified Schematic

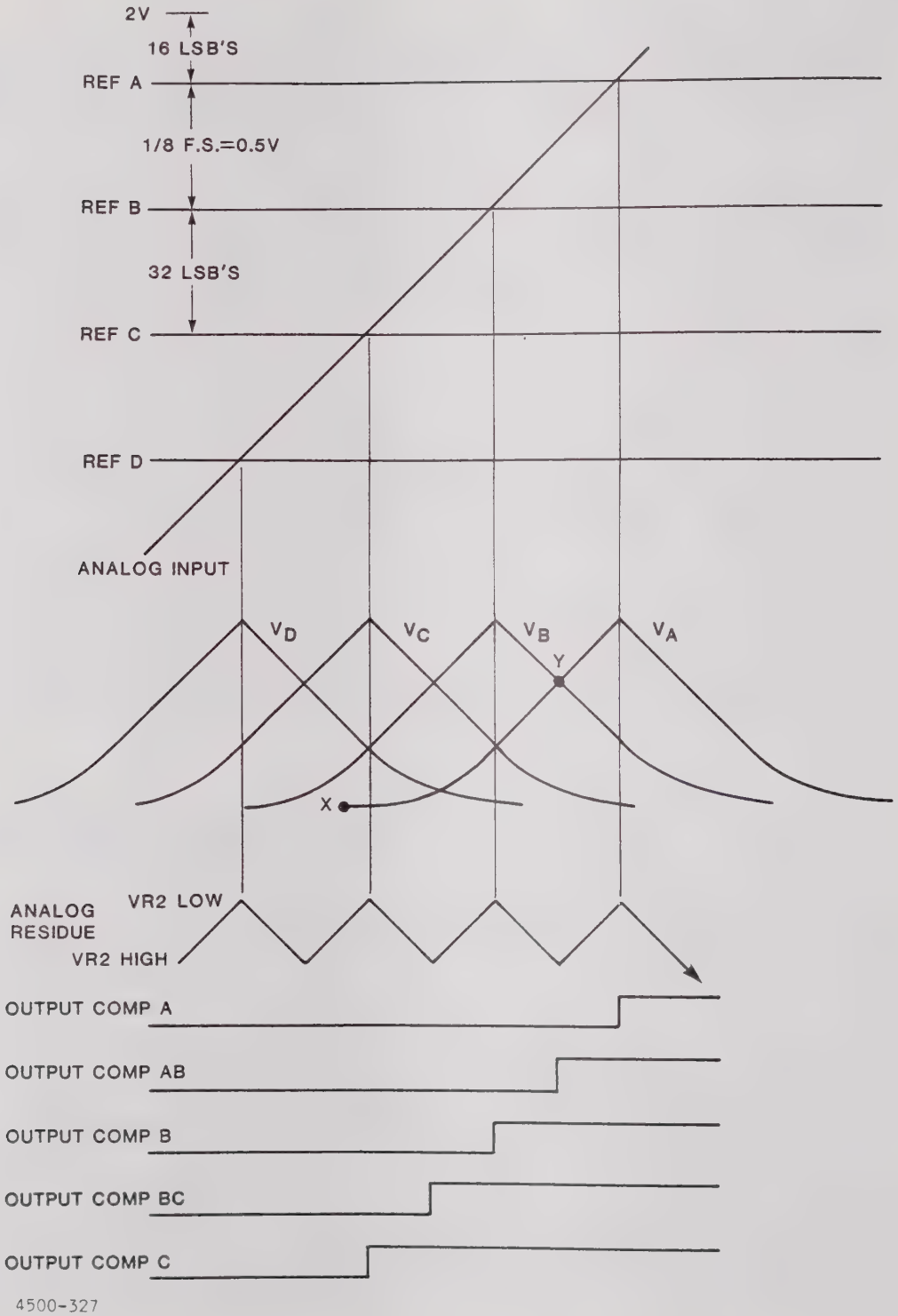


Figure 5-3. Folding Amplifier Array Idealized Waveforms

If the output from comparator #1 is the most positive of all eight comparator outputs, Q57 will take all the current provided by R525, and the other emitter followers will be cut off. The analog residue signal is level shifted and buffered by CR33 and Q59 and then applied to the input of the four-bit flash converter, U40. Comparator #2 is driven by the inphase output of comparator #1 and the antiphase output of comparator #3. It consists of differential pair connected array U70, whose output drives the grounded base PNP pair Q73/72. The other folding amplifiers are similar to the #1 stage.

Folding Amplifier Digital Decode
(Schematic sheet 10)

Differential comparator outputs 1 through 15 are applied to ECL differential line receivers U74, U41, and U19. These in turn are connected to the D inputs of the three flip-flops U75, U42, and U22. The latched output is encoded by NOR U44 and U43 into a four-bit Gray code. The Gray code is applied to a set of final latches (Schematic sheet 11) before going to the Sweep and Record Board.

Four-Bit Flash Converter
(Refer to schematic sheet 6)

U40 contains 16 comparators, a reference chain of resistors, and an encoder, to produce four-bit binary code from the lower fifteen of the comparator outputs. The output is ECL compatible. As the analog signal is increased from the low reference level VR2 LOW (U40 pin 6), toward the high reference level VR2 HIGH (U40 pin 5), the comparators are set in turn to output logic 1 levels, until all fifteen are on. This is internally encoded to binary 1111. If the signal level increases to the high reference level VR2 HIGH, comparator sixteen will turn on. Internal encoding then sets the binary output to 0000 and sets the overflow bit (pin 18) to a logic 1.

The folded analog residue signal applied to pin 4 normally falls within the encoding range of the lower fifteen comparators, and even for signals more positive or negative than the +/-2 volt full scale, the folding action ensures that the residue signal will not be as positive as VR2 HIGH (See Figure 3). During conversion of a high frequency signal however, large scale steps are output by the track and hold circuitry, and ringing may cause the residue to reach the VR2 HIGH level. This causes the overflow comparator in U40 to come on, and the four output bits of U40 to be all zeros. The four output bits being all zeros would cause a 15-bit error in the conversion. To minimize this error, the overflow bit (logic 1) is ORED with each of the four output bits to produce a 1111 result instead of 0000. OR'ing takes place in U79.

Digital outputs from OR U79 are sent to final latches (Schematic sheet 11) before being sent off of the board.

The flash converter U40 has two modes of operation, controlled by the state of the differential latch enable lines L (pin 9) and L* (pin 8). When L is high, a change of analog input causes data changes at the IC output. When L goes low, the data is held fixed.

U40 Pin 15 is the complement of the MSB output which is U40 pin 16. The compliment output (pin 15) is taken via C238 to diode detector CR32, C237, R520. Toggling the most significant bit causes C237 to charge negatively. This voltage is used by comparator U15 pin 4 (Schematic sheet 11) to drive the "in range LED" on the front panel.

ADC Pulse Generator
(Refer to schematic sheet 5)

All conversion system pulses used on the ADC are derived from a single balanced ECL signal that comes from the Sweep and Record board. The conversion rate is set directly by the pulse rate of this input which can be varied over a large range. The maximum pulse rate is 100-MHz. The ADC produces a new output for each positive edge on connector J1, pin 63. The input pulse is transmission-line terminated by R656 and R655 and is applied to differential line receiver U77 pins 22 and 23. The non-inverting output of U77 (pin 5) clocks flip-flop U78 to a logic 1.

The action of U77 (inputs 1 and 24), U45 (inputs 22 and 23), U45 (inputs 17 and 16), and delay line D1 produces a reset pulse for flip-flop U78 so that the output is a 7nanosecond pulse. This is the "hold" drive to the track and hold circuit. Specifically, the 2-nanosecond delayed negative edge from D1 is applied to input pin 24 of U77. The balanced outputs of U77 (pins 2 and 3) are connected to two RC networks. The rate of fall of the negative edge is controlled by R718. The negative output is applied to one input (pin 16) of NOR U45 (pins 10, 11, 16, and 17). The positive edge is delayed by filter R651/C333 and U45 (pins 4, 5, 22, and 23) to the other input of NOR U45 (pins 10, 11, 16, and 17).

The timing of these two inputs causes a narrow positive pulse at output pin 11, which resets U78. The leading edge position can be adjusted by R718. The balanced "hold" pulse from U78 is taken via 100 ohm bifiliar wire to T3 (schematic sheet 4) and terminating resistors R155 and R154. This is at the input of differential pair Q17/Q78 in the track and hold circuit.

The negative edge propagating in 10-nanosecond delay lines D1 and D2 (schematic sheet 5) produces all the other latch pulses for the ADC. A tap at pin 8 of D2 takes the edge to the inverting input, pin 17 of U77. The positive edge at output pin 11 of U77 drives three 33 ohm lines: LS1, LS2, and LS3; which are applied to the clock inputs of first rank latches U75, U42, and U22 (schematic sheet 10).

A tap at pin 5 of D2 (schematic sheet 5) takes the edge to input pin 21 of U77, producing balanced outputs at output pins 8 and 9. The negative edge on pin 8 is taken directly to input pin 20 of OR/NOR U45 (pins 8, 9, 20, and 21). The positive edge from U77 pin 9 is routed via R661 and C338, and non inverting gate U45 (pins 1, 2, 3, and 24) to input pin 21 of U45. The delay between these inputs causes U45 pins 8 and 9 to produce a narrow (approximately 2 nanoseconds) balanced output pulse with pin 8 going positive and pin 9 going negative. This signal is labelled L on the schematic, and is the latch drive to the four-bit flash converter U40 (Schematic sheet 6).

The negative edge propagating in D2 (schematic sheet 5) is applied via tap 8 to input pin 15 of U77, producing the balanced signal DR (data ready) on output pins 12 and 13. This is applied via the edge connector and motherboard to the Sweep and Record board. The output DR also clocks the final latch on the ADC (schematic sheet 11), which latches the full eight-bit data word. Adjustment of the bias applied to pin 14 of U77 (schematic sheet 5) affects the time position of DR relative to the other latch pulses.

The timing of the latches is such that the data clocked into the final latch, is the same data that was clocked into the intermediate first and second rank four-bit latches by the previous input strobe. An analog input signal can be sampled and converted by one strobe, but the data representing that sample will not be presented to the Sweep and Record Board until the negative edge of the next strobe passes through delay lines D1 and D2.

LED Drivers for In Range and Out Of Range Indicators
(Refer to schematic sheets 10 and 11.)

The encoded D4 data line at the output of U44/43 is taken to pin 17 on U22, which is the D input of a flip-flop. The state of this input is clocked to the Q output, pin 5, by clock LS3; which is one of the three first rank latch drives. The output from pin 5, RGD, is AC coupled via C311 to diode detector CR44, R645, and C321; so that toggling of D4 charges C321 negatively.

A similar circuit working on the most significant bit of the second rank, produces a negative charging of C237 for toggling this bit (schematic sheet 6). The signals from C237 and C321 are taken to quad comparator U15. If the voltage on C321 is zero; input pin 8 of U15 will be more positive than the reference level set on pin 9 by R287 and R288; and the output of comparator U15, pin 14 goes low pulling pins 2 and 14 to approximately -5 volts. Similarly, if the voltage on C237 is zero, U15 output, pin 2 pulls pins 2 and 14 low. Under these conditions the voltage on connector J1 pin 76, the "in range" LED drive, will be near zero volts and the LED will be off. If toggling is taking place on both D4 and D5, the voltage on J1 pin 76 will be high, and the "in range" LED will be on.

The other comparators in U15 indicate if the signal in the ADC has gone more positive than the most positive comparator, or has gone more negative than the most negative comparator in the folding amplifier stage. This is done by diode detectors CR45, C328, R646 and CR17, C153, R336 (schematic sheet 10) working on the first rank latched output in U75, and U22. These present signals RD1, and RD3 to U15, and are compared to the reference level at the junction of R289, and R288. If the signal exceeds the prescribed range in the positive direction, output 13 which had been pulled to -5 volts goes positive, lighting the LED driven by the voltage on J1 pin 73. Similarly, if J1 pin 75 goes positive, its associated LED lights to indicate large negative signals in the ADC.

Reference Voltage Generators
(Refer to schematic sheet 9)

The primary reference is U65, a precision +10 volt source, with fine adjustment R561. This is used by one half of dual Op Amp U18 (pins 8, 9, and 10), connected as an inverter, to produce -10 volts. This voltage is buffered by op amp U21 (pins 8, 9, and 10) and Q35 connected in a source follower configuration, to produce the negative supply voltage for the folding amplifiers. The positive supply for the folding amplifiers is similarly produced by op amp U21 (pins 5, 6, and 7) and Q36 using the +10 volt reference as input. The +/-2 volt references for the folding amplifier array are derived from inverting amplifier U21 (pins 1, 2, and 3) and its associated transistor Q33, and U21 (pins 12, 13, and 14) and its transistor Q34.

For the +2 volt circuit, negative feedback around U21 (pins 1, 2, and 3) creates a current balance at pin 2, which is a virtual ground point. Neglecting R321, current from the -10 volt reference through R178 and R200 is balanced exactly by current flowing to the emitter of Q33 through R319. The ratio of R178 plus R200, to R319 is nominally 5 to 1, with variable R178 allowing some adjustment of the +2 output voltage. AC feedback via C141 improves loop stability. Current injected at the virtual ground point by R321 enables slight modification of the reference by the Auto Calibration system. If Auto Cal is off, current in R321 is zero.

The -2 volt reference is similarly derived by U21 (pins 12, 13, and 14) and Q34, using the +10 volt source as input. The ratio R179 plus R201 to R328 is 5 to 1, with R179 adjustable, and Auto Cal adjustment through R330.

Reference circuits for the second rank flash converter are U18 (pins 12, 13, and 14) with Q32, and U18 (pins 1, 2, and 3) with Q31. Reference VR2 HIGH is approximately +1 volt, adjustable by R180. The circuit is similar to the +2 volt reference, using the -10 volt reference as input, and R180 for adjustment. Reference VR2 LOW is approximately zero volts. A similar circuit is used, this time with inputs from both the +10 and -10 volt references, to allow R181 to set VR2 LOW with a +/-200 millivolt range of adjustment. Auto Cal input is via R302.

Currents for the eight folding amplifier input stages are set by quad op amps U12 and U20, and potentiometers R170 through R177. To understand the operation of these current-setting circuits consider the folding amplifier with the most positive reference, U71 (schematic sheet 6). The output of Op Amp U20 (pins 5, 6, and 7); acting through R673, R636, emitter follower U71 (pins 12, 13, 14), R672, and R325; forces the voltage at pin 13 of U71 to be equal to the voltage on the wiper of R177. Adjustment of R177 then controls the current set up in U71 (pins 12, 13, and 14), which is the current source for the differential amplifier. The other seven circuits are similar.

Trigger Generator
(Refer to schematic sheet 12)

The signal picked off the output of the ADC input amplifier (schematic sheet 1) by divider network R49, R663, and R56; is fed to relay K4. If K4 is closed the signal is DC coupled to the input resistor, R351, of the high input impedance trigger buffer amplifier Q37, Q38, and Q39. If the relay is open the signal passes through the AC coupling capacitor C157, to R351. Dual FET Q37 is arranged in a totem pole circuit such that if the FETs were identical, and R352 was equal to R359 plus R360, the voltage at pin 6 of Q37 would be equal to the voltage at pin 3. The signal is then taken to PNP emitter follower Q38 and NPN emitter follower Q39. Adjustment of R360 compensates for FET mismatch and differences of transistor base-emitter voltages, to make the voltage on the emitter Q39 equal to the FET input voltage. The gain of the amplifier is near unity. The signal is then passed via R357 to link W7 and relays K5 and K6.

For the B Channel ADC the relays are not fitted and the link W7 is not cut. For the A Channel ADC the relays are fitted and the link W7 is cut. This is because the external trigger signal from the external trigger buffer amplifier is applied to J3 of the A Channel ADC only, so that it is only on this channel that the selection between internal and external trigger is required.

Processor control ensures that only one of the trigger sources is connected via K5 or K6 to compensation network C160/R362. The signal is then passed by K7 or C163 to the inputs of the comparators U26 and U27. For the LF reject option, K7 is open and C163/R680 form a high pass filter. For DC coupling, K7 is closed. If HF reject is selected, K8 is closed, and C164 is placed across the signal path, forming a low pass filter with series resistors R362 and R357. The signal is then applied via R378 and R377 to the inputs of two fast comparator circuits U26 and U27.

U26 is driven on its non inverting input, with positive feedback applied via R331 and R375 to the inverting input. The DC voltage on the inverting input is set by DAC U24, and op amp U25 (output pin 7) acting via R374. If input pin 2 becomes more positive than input pin 3, output 8 will go negative, feeding back a regenerative negative signal to pin 3, causing a rapid switching of the output state. To make the output change back, the input voltage on pin 2 must move negative by the hysteresis range set by the output swing at pin 8 divided by the feedback ratio of R381 to R375. This action prevents oscillation of the comparator, generating a single output step as the trigger signal crosses the trigger threshold set by DAC U24.

The action of U27 is similar, except that the signal is applied to the inverting input, feedback is from the non inverting output to non inverting input, and the trigger level is set by U24 and U25 (output pin 1).

The two outputs of U25 are out of phase; that is: if +10 volts is on pin 7, there will be -10 volts on pin 1. The outputs of the two comparators, U26 and U27, are ECL levels and are connected to ECL gates U28, U29, and U30. These gates enable the selection of four trigger detection states: edge, enter band, leave band, off. Edge trigger occurs when a trigger output is generated by the crossing of the trigger level by the signal at the input of U26. This happens for either positive or negative slope. The selection of positive or negative slope triggering is determined by the set up of exclusive NOR U28.

Enter Band triggering occurs when the signal enters from the positive or negative direction. The symetrical levels around ground; set up at the inputs U26, and U27; are set by the two outputs of U25.

Leave Band triggering occurs when the signal leaves the band set up by the outputs of U25 in either direction. Selection of enter or leave band triggering is determined by the state of Exclusive NOR U28.

For positive Edge triggering the function of the gates is as follows: The signal generated at output pin 7 of U26 is taken to one input (pin 14) of the exclusive NOR U28. When pins 15 and 5 of U28 are low (this occurs when positive edge or leave band triggering is selected), the Exclusive NOR gates become inverters, so that the positive trigger edge from U26 is inverted at output pin 12 of U28, and non-inverted at output pin 14 of U29. U28 pin 14 drives either J1 pin 78 or input pin 6 of U30, depending on the link connections W6 and W2.

For leave band triggering, the positive edge from either U26 or U27 causes output U29 pin 9 to go positive, output U28 pin 2 to go negative, and output U29 pin 3 to go positive. U29 pin 3 is connected to either J1 pin 77, or pin 4 of U30, depending on the link connections W1 and W5.

For negative edge or enter band triggering, U28 is set to its non-inverting mode.

The A Channel ADC has links W5 and W6 closed and links W1 and W4 open. The trigger signals are taken from J1 pin 77 and J1 pin 78, via the motherboard, to J1 pin 77 and J1 pin 78 on the B Channel. As links W3 and W4 are made on the B Channel, the trigger edges generated on the A Channel are applied to inputs 5 and 7 of U30 on the B Channel, giving complimentary outputs at J1 pin 61 and J1 pin 62. This balanced ECL signal is taken via the motherboard to the Sweep and Record Board.

The B Channel has links W1 and W4 closed; links W5 and W6 open. The trigger signals at the outputs of U29 are therefore taken directly to input pins 4 and 6 of U30, again giving a balanced output at J1 pins 61 and 62.

The comparison levels used by U26 and U27 are derived from an eight-bit DAC, U24, whose data lines are driven by data latch U49 (schematic sheet 12). Input pin 6 of op amp U25 is a current summing point. With all digital inputs of the DAC, U24, low; the current flowing into pin 4 of U24 is zero; and the 1 milliamp through RP32, pins 5 and 4 is balanced by 1 milliamp in RP32 pins 3 and 6. This causes a -10 volt output at pin 7 of U25. With all digital inputs of the DAC high, the current into pin 4 of U24 is 1.992 milliamps, making the op amp respond with an output voltage of approximately +10 volts to maintain the current balance. Resistor R366 provides the 2 milliamp reference for U24 from the +10 volt reference supply.

Input Offset and Offset AUTO CAL
(Refer to schematic sheet 13)

The offset voltage used by the input attenuator and buffer amplifier is generated by a 12-bit DAC U62 and dual op amp U60. DAC U62 contains a single R/2R ladder whose shunt elements are switched by data inputs, either to pin 1 or to pin 2. For correct operation, pins 1 and 2 must be virtual ground points within 1 millivolt of pin 3. Feedback around U60 from output pin 12 through R541 and RP2 (pins 4 and 5) to inverting input pin 1, and from output pin 10 through U62 to inverting pin 7, makes inputs 1 and 7 virtual ground points. R540 and R539 are used to balance out the input offset of U60 to less than 1 millivolt. Current flowing out of U62 pin 2, is balanced by current flowing toward output pin 12 of U60 through RP2 (pins 4 and 5).

With the applied reference of +10 volts on pin 17, the current on pin 2 of U62 is set to 1 milliamps for digital input of all zeros, and to 0 milliamps for a digital input of all ones. This results in output pin 12 of U60 being set in the range 0 to -10 volts by the digital input code to the DAC.

The current provided by the R/2R resistor elements internal to U62 is the feedback current around U60 (pins 6, 7, and 10). This current is equal to the current from output pin 12 of U60 flowing through RP2 (pins 6 and 3), and results in output U60 pin 10 being set in the range -10 to +10 volts by the digital code into U62.

The +/-2 volt offset source for the input attenuator and buffer amplifier is derived from U60 pin 10 by the potential divider consisting of R542, R538, and R544. This is taken via CMOS analog switch U61 to J4, which connects to the ribbon cable going to the Attenuator. During the Auto Cal routine an absolute ground reference is provided for the input attenuator circuitry by opening switch U61 pins 8 and 9, and closing U61 pins 4 and 5. The unattenuated signal at U60 pin 10 is taken directly to the attenuator via J4, were it is used by the calibration system. It is also taken to a unity gain buffer on the keyboard, and the buffer output drives the CAL test point on the front panel.

The digital inputs for DAC U62 are latched from the data bus by U51 and U52. The +/-2 volt offset sent to the attenuator can be altered slightly under the control of the microprocessor, for Auto Calibration. If an offset error is detected by the system, an eight-bit DAC, U48 provides correction. The current into R534 is the sum of the DAC output current (U48 pin 4) and 0.5 milliamps through R533, yielding a digitally controlled voltage swing at pin 4 of +/-10 millivolts. This is one end of the offset potential divider, so that the offset can be changed by about this +/- 10 millivolts. Data for U48 is latched from the data bus by U50 .

Correction for gain errors found by the calibration system are done through eight-bit DAC U57. This generates two complimentary output voltages at pins 4 and 2. With all logic ones applied, output 4 will be -10 volts, and output 2 will be +10 volts. With all logic zeros applied, output 4 will be +10 volts, and output 2 will be -10 volts. These voltages, acting through dual unity gain buffer op amp U23 (schematic sheet 9), modify slightly the +/-2 volt reference for the folding amplifiers by injecting currents into the summing nodes of the reference generators through R321 and R330. The low reference for the second rank is also effected via R302. Input data for DAC U57 is latched by U56 from the data bus.

The inputs for the trigger level DAC U24 (schematic sheet 12) are provided by latch U49 from the data bus. Analog switch U61 is controlled by two outputs from data latch U52.

Data latches U51, U53, and U54 directly drive the reed relays used in the input attenuator via connector J4. These latches also drive the relays used for 1/2/5 attenuation on the ADC board (schematic sheet 1).

The signals that control band or edge triggering, and leave or enter band triggering, come from latch U54 (schematic sheet 13). TTL to ECL level converter U46 converts these signals to ECL levels. Band triggering is activated by the signal BAND*, edge triggering is activated by the signal EDGE*, and leave or enter band triggering is selected by the signal L*/E.

Data is presented to the data flip-flops U49 through U54, and U56, in the following manner: Processor lines A4 through A7, I/O, and WR*; acting on the binary inputs and enables of 1-of-8 decoder U59 (schematic sheet 13); causes output pin 11 (channel B) or output pin 12 (channel A) to go low if one of the ADCs is addressed. This enables the outputs of U55, a three state octal buffer, and bus data is placed on the inputs of the flip-flops. Address lines A0 through A3, and an output from U59, act on the inputs of one of eight decoder U58, so that one of its outputs (U58 pins 9 through 15) goes low. This takes the clock input of one of the flip-flops low. When WR* goes high, the flip-flop clock goes high, and clocks in the data.

Power Supply
(Refer to schematic sheets 1 and 9)

The +18 volt supply (schematic sheet 1) is taken through filter L12, C277, and C276, to the input of adjustable regulator U64. The regulator compares the voltage across the top arm of the potential divider made up of R551, R553, and R552; to its internal 1.2 volt reference. This sets the voltage across R551 to 1.2 volts, and the output voltage across C271 to +15 volts. CR36 is a protection diode. All other positive supplies on the ADC are derived from the +15 volts.

The negative regulator is similar. The input filter is L11, C267, C268 and the 1.2 volts is set across R550. The output across C270 is -15 volts, and is used to derive all the other negative supplies on the ADC.

The +6 volt supply for the second rank four-bit flash converter comes from series regulator Q61, with its reference CR37 (schematic sheet 9). This regulator uses the +15 volt supply as its input.

The +12 volts required by the between section comparators in the folding amplifier array (schematic sheets 6, 7, and 8), is marked Vbc on the schematic (schematic sheet 9). Vbc is provided by the potential divider made of R204 and R205, and emitter follower Q18. This supply also uses the +15 volt supply as its input.

The +/-10 volt supplies (schematic sheet 9) for the folding amplifiers have been described in the Reference Voltage Generators section.

ATTENUATOR BOARD THEORY OF OPERATION
(Refer to schematic 0285-0301)

The following paragraphs describe the theory of operation for the Attenuator Board at the detailed schematic level.

Introduction

The Attenuator board contains three separate circuits: (1) the channel A passive attenuator and buffer amplifier, (2) the channel B passive attenuator and buffer amplifier, and (3) the external trigger attenuator and buffer. Channel A and channel B circuits are identical. Component reference designations for channel B are given in the text in parentheses.

Channel A and Channel B Passive Attenuators

The attenuator has a 1 Megohm, 30pF input impedance on all ranges. There are three sections. These divide the input voltage by 1, 10 or 100. The terminating resistor is R19 (R56), which on the divide by 1 range provides the 1 Megohm input impedance. The divide by 10 section consists of R8 and R7 (R53 and R52), which form an L attenuator with the terminating resistor. Similarly the divide by 100 section consists of R4 and R3 (R49 and R48).

Attenuation is maintained constant for high frequency signals by capacitive compensation. Capacitor C7 (C39) is adjusted for correct response of the divide by 10 section, and C16 (C48) is adjusted for correct response of the divide by 100 section.

The input capacitance of each section, is maintained at 30pf by adjustment of C10 (C42) in the divide by 1 section, C5 (C37) in the divide by 10 section, and C12 (C44) in the divide by 100 section.

Reed relays select the various sections. A signal applied to the input BNC connector is routed through AC coupling capacitor C18 (C50), which is bypassed for DC coupling by closing relay K4 (K12). The signal is then passed via K3, K2, and K1 (K10, K11, and K9), to the input of the divide by 1, divide by 10, and divide by 100 sections respectively. The output of the selected section is then connected via either K6, K5, or K7 (K14, K13, or K15) to the buffer amplifier input.

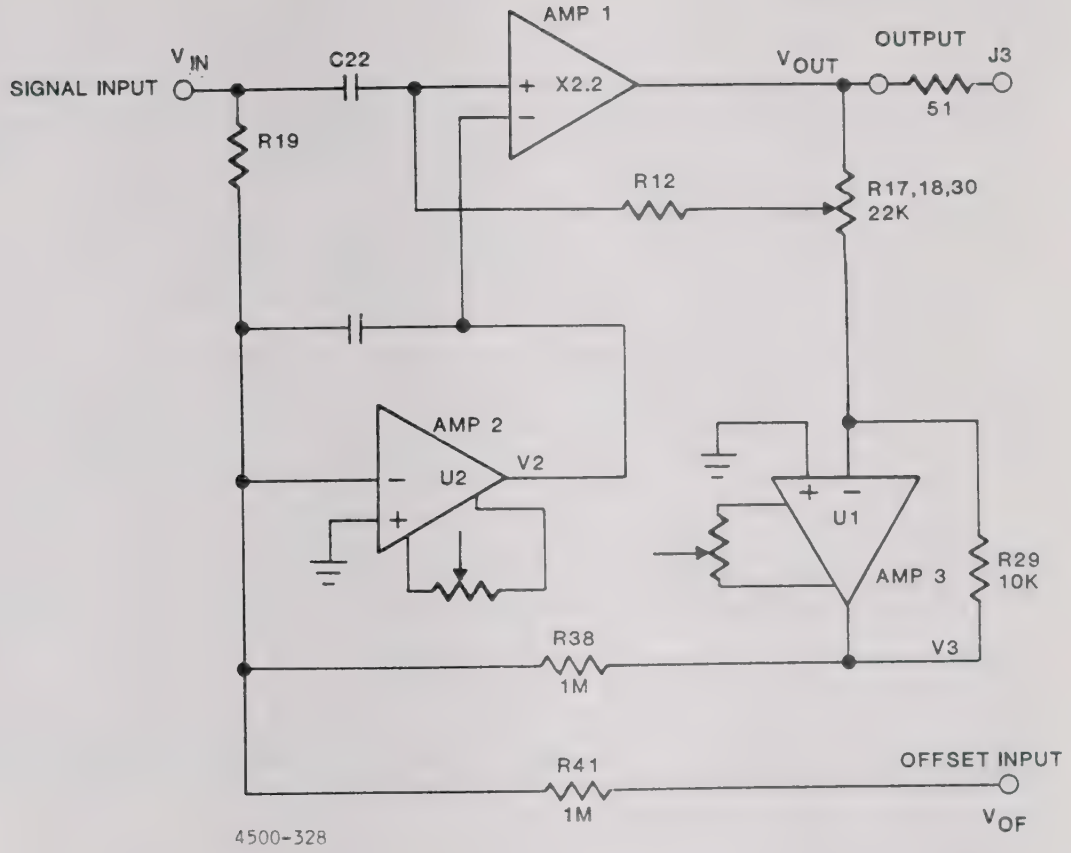
The calibration signal, used in the automatic calibration procedure, is applied through the divide by 100 section to the amplifier input by closing only K8 and K7 (K16 and K15). The relays are driven directly by TTL logic on the ADC board through a cable connected to J1 (J2).

Channel A and Channel B Buffer Amplifiers

The amplifier has an input impedance of 1M ohm set by R19 (R56), a bandwidth greater than 50-MHz, and a gain of 2.2 when no load is applied to its output, and an output impedance of 50 ohms. It drives a coaxial cable which is terminated in 500 ohms on the ADC board. Therefore the gain from the input of this amplifier to the ADC board is 2.0.

Referring to the simplified schematic of the input attenuator buffer, Figure 5-4, Amp 1 is an FET input high speed DC coupled amplifier with a gain of 2.2. Its DC stability with temperature is inadequate, and it is one of the functions of operational amplifiers Amp 2 and Amp 3 to correct this. Consider the signal and offset input voltages to be zero, and the two op amps to be balanced correctly. If the output voltage Vout is not zero, but X volts, V3 will be -X divided by 2.2. This is because the gain of this amplifier is set by the ratio of R29 which is 10K, to the total of R17 plus R18 plus R30 which is 22K. This voltage applied though R38 to the input of Amp2 (which has a gain of greater than 100,000) will give a sufficiently large output to the inverting input of Amp1, to ensure that X must be very small and determined only by the balance of Amp2 and Amp3.

If the voltage on the signal input is suddenly changed by 1 volt, the output of Amp1 will become +2.2 volts within a few nanoseconds, and the output of Amp3 will become -1 volt within a few hundred nanoseconds. The inverting input of Amp2 acts as a summing node for the currents in R19, R38, and R41. In this case the balance is exact, and the input and output voltages of Amp2 will not be altered by the change of signal input voltage.



4500-328

Figure 5-4. Input Attenuator Buffer Simplified Schematic

Any unbalance, due to slight gain errors in Ampl, will cause Amp2 to produce a correction voltage that reduces the input voltage of Amp2 to essentially zero volts. Its input can be considered a virtual ground point. R12 is tapped into the potential divider chain R17, R18, and R30 at the unity gain point; so the voltage across C22 remains constant for changes of signal input voltage. If a voltage is applied to the offset input, Amp2 output will be altered such that working though Ampl, the output of Amp3 responds with an equal and opposite voltage, maintaining the current balance at the input to Amp2. Therefore, for +1 volt applied to the Offset Input, + 2.2 volts will appear at the output of Ampl, and the voltage across C22 will be changed by 1 volt.

Description of Amp 1

Ampl is a feedback FET input amplifier with a non inverting gain of 2.2. With no signal or offset inputs applied, the action of U1 and U2 is to ensure zero voltage at the output, R16 (R79), as described previously. The current through FET Q2 (Q8) is then determined by R13 and R14 (R59 and R58) to be approximately 7mA. This current flows through Q3 (Q9), whose base is held at 6.8 volts by zeners CR4 and CR9 (CR18 and CR14). The inverting input of Ampl is the base of Q7 (Q14) which is driven by U2 (U4). As the base is driven more positive, current in this transistor and in Q5 (Q10) is increased so that in normal operation the current in Q5 (Q10) is equal to current in Q3 (Q9), neglecting the small base current of Q4 (Q11).

Transistor Q4 (Q11) is a PNP current-to-voltage amplifier whose load is R24, and Q1 (Q12) is an emitter follower from the collector of Q4 (Q11) that drives the output via zener CR4 (CR18). Feedback is via R14 (R58) to the source of the FET Q2 (Q8). The gain of Q4 (Q11) is high enough that the overall gain is set by R13 and R14 (R59 and R58) and is (R14 + R13)/R13. Due to the high internal gain, any normal output voltage can be produced by Q4 and Q1 (Q11 and Q12) with only a very small change in FET current. The FET gate-to-source voltage is also held constant for changing input voltage by the potential divider formed by R25 and R22 (R60 and R63) acting on Q3 (Q9).

Transistor Q6 (Q13) is a current source for the emitter of Q1 (Q12). Input protection against high voltage is provided by diodes CR1 and CR6 and zener CR9 (CR12, CR13, and zener CR14) in the positive direction; and by CR5, CR6, and zener CR11 (CR15, CR17, and zener CR16) in the negative direction. Local feedback via C80 and C23 (C81 and C56) sets the pulse response of the amplifier.

External Trigger
(Schematic sheet 3)

Trigger signals applied to the BNC connector are routed through AC coupling capacitor C75, or for DC coupling through relay K17, to the 1 M ohm attenuator formed by R92 and R94. The input capacitance of the buffer amplifier and C74 form a capacitive attenuator which maintains the attenuation ratio constant for high frequency signals. The attenuator input capacitance of 30pF is set by C71 and C73. The attenuation multiplies external trigger inputs by a factor of 0.365.

The output of the attenuator is applied to the input of the buffer amplifier. Dual Matched FETs Q17 and resistors R99 and R102 are connected in a totem pole configuration. If the FETs were identical, and the resistors equal, the voltage on drain (Q17 pin 6) would be equal to the gate voltage (Q17 pin 3). The FET feeds the two emitter followers Q15 and Q16, the base-emitter voltages of which approximately cancel. The DC output voltage at the emitter of Q16 may be made equal to the input FET gate voltage by adjustment of offset potentiometer R101, which compensates for mismatches in the FET and resistors R99 and R102. The buffer amplifier has a gain of almost unity.

Protection against high input negative voltages is provided by CR24 and CR23. High positive input voltages are clamped at the buffer amplifier input by conduction of the gate-drain diode of the input FET. CR25 protects Q15 from a large emitter-base reverse bias.

The signal from the emitter of Q16 is taken via R104 and connector J5 to a coaxial cable which goes to the A channel ADC.

INTERFACE OPTIONS BOARD THEORY OF OPERATION

(Refer to schematic 0285-0061)

The following paragraphs present the detailed theory of operation for the Interface Options Board.

Microprocessor Interface

(Refer to schematic sheet 1)

The RD*, WR* and address lines are buffered by U10D and U11D. The outputs of the buffers are decoded by U6D, U7D, U8D, and U9D to enable reading from and writing to various circuits on this board. Data to and from the microprocessor is routed via transceiver U9C.

RS-232 Interface

(Refer to schematic sheet 1)

The RS-232 interface consists of U5B, a programmable timer that generates different clocks for various baud rates; and U3B, a programmable communication interface that reads and writes the RS-232 signals. The RS-232 signals are buffered by U1B and U1C. These are necessary to interface with the +/- 15V levels used in the RS-232 system.

GPIB Interface

(Refer to schematic sheet 2)

GPIB data comes in and goes out of Interface Options circuit board on connector J10 pins 43 through 50. This data is labelled DIO1 through DIO8. The data out is driven by U4D and U5D, and the data in is buffered by U3D.

GPIB control signals come in and go out on connector J10 pins 30, 32, 34, 36, 38, and 40. These signals are labelled ATN, SRQ, IFC, REN, EOI, NRFD, NDAC, and DAV. The three wire (NRFD, NDAC, and DAV) handshake is performed by U4A, U5A, and U8A.

The MPU is interrupted by the signal INTRO from U3A, pin 3. This interrupt is generated when any of the following conditions occur:

- when a listener interrupt comes from the GPIB, telling the MPU that data is ready on the bus (LINT is generated at U7A pin 13);
- when a talker interrupt comes from the GPIB, telling the MPU that the bus is ready for us to put data onto it (TINT is generated at U7A pin 12);
- when the interface clear (IFC) signal from the GPIB comes true, telling the MPU to set the interface to a cleared state (CLINT is generated at U7A pin 10),
- or when the remote enable (REN) signal from the GPIB comes true telling the MPU that the GPIB controller is not active and that the 4500 must revert to local rather than remote mode (NRINT is generated at U7A pin 9).

The ICL signal (U11A pins 1 and 13) is generated by the MPU and clears the GPIB interface circuitry on this board.

DMA Interface
(Refer to schematic sheet 3)

The DMA interface consists of two parts. These are the analog averager output, and the PDP-11 compatible DR11-B output. Descriptions of these follow.

Analog Averager Output
(Refer to schematic sheet 3)

The analog averager output uses U12B, an NE5018 digital-to-analog converter (DAC) to generate the analog averager output. The analog output voltage and the analog output ground leave the board on J10 pins 2 and 4. The digital data to be converted to analog comes from the Sweep and Record board, and enters the Interface Options board on J5 pins 35 through 42. This digital information is first converted to unsigned binary by PROM U14B. The converted binary is clock-ed into U13B, and the outputs of U13B are the digital inputs to the DAC.

When the analog averager output is selected to be active, the MPU raises the signal ANALOG OUT ENABLE which is the output of U16B, pin 9. This signal high causes the outputs of U17C, pins 6 and 12, to be high; and the output of U17C, pin 8, then becomes a 200 kHz clock. This clock is used to request new data from the Sweep and Record board, via the READ DIRECT signal which leaves the Interface Options board on connector J5 pin 34; and to clock the previous data from the Sweep and Record board into U13B.

The 200-kHz clock is generated by decade counter U18B. This counter is enabled by the ACCESS ENABLE signal being high. The ACCESS ENABLE signal is set high by the MPU when the DMA output is selected to be active. This is done by the MPU pulsing the GO* signal to a low. This signal is applied to the input of NOR gate U16D, pin 8, and also to the trigger input of monostable U18D, pin 1. This action causes the input to flip-flop U17B, pin 3 to go high; which causes the output of U17B, pin 9 to go high. U17B, pin 9 is the signal ACCESS ENABLE.

DR11-B Output
(Refer to schematic sheet 3)

This circuitry operates with a Digital Equipment Corporation DR11-B general purpose DMA interface. Data is provided to the DR11-B interface via connector J10 pins 17 through 24. The interface control lines are CYCLE REQUEST, BUSY*, READY*, and BURST/SINGLE*. These are sent or received via connector J10 pins 16, 15, 12, and 10 respectively.

To enable this interface the microprocessor lowers the ANALOG OUT ENABLE signal and pulses tne GO* line which causes the ACCESS ENABLE signal to become high as described in the ANALOG AVERAGER OUTPUT section above.

The DR11-B interface may operate in one of two modes. These are single mode and burst mode. In single mode, the CYCLE REQUEST signal is sent out each time a data byte is to be transmitted, and the DR11-B interface responds with a BUSY* pulse for each byte. In BURST mode, CYCLE REQUEST is sent out once, and then a byte is sent for each BUSY* pulse with no further CYCLE REQUEST pulses being issued.

In single mode the BURST/SINGLE* signal is low and gate U17C pin 12 is forced high. Gate U17C pins 3, 4, 5, and 6 is active. BUSY* is initially high and CYCLE REQUEST is initially low. CYCLE REQUEST is caused to go high by output pin 5 of flip-flop U17D. The DR11-B interface then responds by bringing BUSY* low. This will cause U17D pin 5 to go low. After the data transfer, BUSY* will go high to complete the cycle. New data is obtained from the Sweep and Record board each time U17D pin 5 goes high. This is via the READ DIRECT signal on J5 pin 34.

In burst mode the BURST/SINGLE* signal is high and gate U17C pin 6 is forced high. Gate U17C pins 1, 2, 12, and 13 is active. BUSY* is initially high and CYCLE REQUEST is initially low. CYCLE REQUEST is caused to go high by output pin 5 of flip-flop U17D. The DR11-B interface then responds by bringing BUSY* low. This does not cause any change of the output of U17D pin 5, and CYCLE REQUEST stays high. BUSY* pulses occur for each data transfer and are used to obtain new data from the Sweep and Record board via the READ DIRECT signal on J5 pin 34. Flip flop U17D pin 5 is reset after all data is transferred, by the microprocessor raising the ANALOG OUT ENABLE signal.

The control of write precompensation timing is determined by the PS0 and PS1 lines (pins 32 and 31) of the 8272. ICs U5E and U6E implement the precompensation. Shift register, U5E passes the write data at a 125-nanosecond rate. The shift register has three outputs (pins 5, 7, and 10). Any of these can be selected by data selector, 6E. Control lines PS0 and PS1 determine whether data is written early, normal, or late relative to when it is sent out of the 8272.

Digital Data Separator

The Digital Data Separator uses a digital phase locked loop to separate the clocks and data coming from the floppy disk drive. PROM, U8A is programmed so that, when used with U7A, it is self addressing. The clock input to U7A, pin 9, clocks the phase locked loop. At each clock pulse the data at the last address becomes part of the next address. PROM address input A4, (U8A pin 3), is an additional address input that is the read data from the disk drive, routed via U6B pin 3, and U7A pin 3. When no read data is coming from the disk drive the PROM runs in a loop. That is, the data out of the PROM creates addresses into the PROM that stay within a limited range of numerical values.

When a read data pulse comes into address input A4, the PROM output data sends addresses into the PROM that are in a different numerical range. This numerical range, and the data the PROM generates, define a different type of phase locked loop operation as follows: the read data is a string of ones and zeros. Some of these bits are data bits, and some are clock bits. Due to the data encoding scheme there will always be bit changes (representing clocks or data) at approximately a constant rate. The rate does vary however, because of disk drive motor speed changes. The PROM, expecting a bit stream waveform with a 4-microsecond nominal period (i.e., a pulse every 4 microseconds with some missing pulses), will be able to lock onto the expected pulse pattern. It does this by causing its data out, when a zero is input to address input A4, to be greater than its address in. This drives the next data out, and therefore the next address in, in a continuous loop.

When a logic "1" comes in on address line A4, the data/address interaction drives the address toward a value, that once reached, stays constant.

The outputs of the data separator are the read data that enters the 8272 on pin 23, and the data window signal that enters the 8272 on pin 22.

Clock Generator

The board clock is generated by a 74LS629, U9B; and an 8-MHz crystal, Y1. The 8 MHz is divided down to produce 4 MHz at the output of U7C, pin 5; and divided further to produce 1 MHz, 500 kHz, and 250 kHz at the outputs of U8C. The write clock that is input to the 8272 on pin 21, is developed by U7C (output at pin 9), and U6A (output at pin 5). This clock is a 125-nanosecond pulse at a 500-kHz rate.

The circuitry is designed to operate a floppy disk drive in the FM or inthe MFM mode. These modes require different clock frequencies, and U8B makes the desired clock selections. The 4500 always operates in the MFM mode.

Disk Drive Power

The floppy disk drive requires 12 Vdc for its operation. An LM350 voltage regulator, Q1, provides this power. The 12 Vdc is derived from the instrument +18 Vdc power supply.

FRONT PANEL THEORY OF OPERATION

(Refer to schematic 0285-0026)

The following parargraphs provide the detailed theory of operation for the Front Panel of the 4500.

Key and Rocker Switches

Each front panel pushbutton key has a snap dome under it, and each rocker switch has two snap domes under it in each direction of travel. When depressed, the snap domes make contact with a trace pattern on the front panel keyboard and act as a switch by shorting traces. The collection of front panel switches are grouped in a matrix. Each row in the matrix may be activated individually by the microprocessor (MPU) and the columns may be read by the MPU. Any switch, when depressed, will result in a logic zero being read by the MPU, in the column that corresponds to that switch, when the row containing the switch is activated. Each row corresponds to one of the outputs D0 through D15 of U1 and U2. Each column corresponds to one of the inputs of U3.

Clicker

The clicker is a piezoelectric transducer that is caused to click by the MPU when keys or rockers are depressed. The MPU clicks the clicker by reading from a particular address that causes U2 pin 7, and the Read Keyboard signal to both go low. This triggers U7, the output of which drives the clicker.

Front Panel Test Points

On the front panel are three hook on loop test points. These are a squarewave output, ground, and a cal ramp output used for calibrating probes. The squarewave is generated by U5. Ground is connected to ground on the front panel circuit board. The cal ramp comes from a DAC on the channel B ADC board (refer to ADC schematic 0285-0340 sheet 13) via a buffering op amp on the front panel.

Range LEDs

The light emitting diodes on the front panel are driven by U4. The signals that drive U4 come from the ADC boards (ADC schematic 0285-0340 sheet 11). These LEDs indicate if the signals being digitized by the ADC are above, or below, or within the voltage range that the ADC can digitize.

CRT DRIVER BOARD THEORY OF OPERATION

(Refer to schematic 0285-0051)

The CRT Driver provides the drive current for the CRT deflection coils, the high voltage power supply for the CRT, and the CRT grid/cathode control that adjusts display brightness and produces the video information.

Vertical Sync System

Sync amplifier, U6 buffers and shapes the vertical and horizontal sync signals. The vertical sync pulses set the operating frequency of the vertical phase locked loop, U7 to the vertical sweep rate of 33.6 kHz. The output pulse of U7, pin 1 is buffered by transistor Q8 and transformer T2 to provide base drive to the vertical output transistor Q9. When transistor Q9 turns off, a linear current flows in the vertical deflection coil to produce a linear vertical deflection.

High Voltage Power Supply

The high voltage power supply is a resonant deflection system composed of transformer T4, the vertical deflection coil, the vertical height coil L4, and the linearity coil L3. The traditional "S" shaping capacitor is replaced by integrator U8. The nominal anode supply voltage is 12 kV.

Horizontal Oscillator and Driver

The horizontal oscillator and driver, U5 is a TDA1170. This IC provides a 60-Hz deflection voltage to its own power amplifier, which drives the horizontal deflection coil via its output, pin 4. The coil current is sensed by resistor R44 and fed back to U5. Linearity correction is provided by the RC network connected between pins 1 and 12 of U5.

Pin Cushion Correction

The horizontal deflection current feedback is used for pin cushion correction. The 60-Hz ramp is amplified and supplied to two integrators, U1 and U2. U1 integrates for a vertical scan period and then resets. The output is a ramp with an amplitude proportional to the vertical distance that the electron beam is from the center of the CRT screen. After buffering in U3 and U4, this signal is injected into the horizontal deflection circuit via transformer T1. This transformer appears to U4 as an inductor and the correction signal is therefore integrated again. A paraboloid is created with signal polarity changing as the sweep crosses center screen.

Integrator U2 integrates over the horizontal sweep period, also creating a parabolic waveform. This signal is buffered by transistor Q3, which drives transformer T3. Transformer T3 injects a signal opposing the vertical sweep, therefore reducing height as a function of horizontal position.

Video Amplifier

The video amplifier consisting of transistors Q7, Q10, and Q11 amplify the TTL video input signal and drive the CRT cathode.

Intensity Control

The display intensity is controlled by varying the CRT control grid voltage, via the INTENSITY potentiometer on the front panel.

POWER SUPPLY THEORY OF OPERATION

(Refer to schematic 0285-0011)

The 4500 power supply is a half-bridge, switching type. It consists of seven functional blocks.

Input Rectifier Filter

(Refer to schematic sheet 1)

The input rectifier filter rectifies and filters the AC line to provide + 175 V nominal to the chopper. This circuit operates as a voltage doubler in the 120 Vac input mode, and as a full wave bridge in the 240 Vac input mode. Ahead of the rectifier is a line filter which prevents the power supply from radiating RF noise out of the power input.

Housekeeping Supply

(Refer to schematic sheet 1)

Plus and minus 15 Vdc are generated by T1, Q1, and VR1 in the housekeeping supply; and are used by other power supply circuitry.

Pulse Width Modulator

(Refer to schematic sheet 2)

This circuit provides a 20-kHz drive, to the chopper, with a variable duty cycle to keep the -5.2 Vdc output constant. The modulator, U8 is a TL494 integrated circuit. Its outputs are buffered by Q7, Q6, T4 and T5 to provide an isolated base drive to the chopper.

Chopper
(Refer to schematic sheet 2)

The chopper stage consists of Q7, Q8, and associated circuitry. Q7 and Q8 are driven by the pulse width modulator to create a ± 175 V excitation across T6. The diodes and inductors associated with Q7 and Q8 are snubbing and antisaturation circuits.

Transformer T6
(Refer to schematic sheet 2)

Transformer T6 has three center tapped secondaries. When the primary is driven by ± 175 V, the secondaries yield ± 48 Vac peak, ± 8.7 Vac peak, and ± 13 Vac peak. These outputs are rectified and filtered to provide ± 21 Vdc, -3 Vdc, +6 Vdc, and -5.2 Vdc.

Post Regulator
(Refer to schematic sheet 3)

The ± 21 Vdc, -3 Vdc, and +6 Vdc are post regulated by Q16, Q14, Q18, and Q20; providing +18 VDC, -18 Vdc, -2 Vdc, and +5 Vdc. Each voltage is adjustable and has current limiting.

Status Circuitry
(Refer to schematic sheet 4)

The power supply outputs are monitored by the status circuitry. If an output is subjected to an overcurrent, the pulse width modulator is inhibited by the action of U2, U5, U6, and U11. If the AC input is less than 85 Vac, the modulator is also inhibited.

The 17 V generated in the housekeeping supply is shaped by R1, C25, and Q13 to create the line sync signal used for line triggering. U10 and Q10 generate the RESET* signal used to reset the microprocessor and other circuitry.

CHAPTER 6 SCHEMATICS AND REFERENCE DRAWINGS

INTRODUCTION

This chapter contains the schematics, list of materials, and assembly drawings for the 4500 in the following order:

Front Panel

Front Panel Board Schematic	0285-0026
Front Panel Board Assembly Drawing	0285-0025
Front Panel Board List of Materials	0285-0025
Front Panel Assembly List of Materials	0285-0105
Front Bezel Assembly Drawing	0285-0105

Chassis Assembly

Top Assembly Drawing	0285-0002
Top Assembly List of Materials	0285-0002
Chassis Assembly Drawing	0285-0019
Chassis Assembly List of Materials	0285-0019
Rear Casting Assembly Drawing	0285-0214
Rear Casting List of Materials	0285-0214
CRT Assembly List of Materials	0950-0131
Handle Assembly List of Materials	0111-0016
Handle Assembly Assembly Drawing	0111-0016
Mother Board Assembly Drawing	0285-0020
Mother Board Assembly List of Materials	0285-0020
Mother Board Schematic	0285-0021
CRT Intensity Board Assembly Drawing	0285-0130
CRT Intensity Board List of Materials	0285-0130
CRT Intensity Board Schematic	0285-0131

MPU Board

MPU Board Schematic	0285-0046
MPU Board Assembly Drawing	0285-0045
MPU Board Assembly List of Materials	0285-0045

CRT Board

CRT Driver Board Schematic	0285-0051
CRT Driver Board Assembly Drawing	0285-0050
CRT Driver Board List of Materials	0285-0050

Sweep and Record Board

Sweep and Record Board Schematic	0285-0261
Sweep and Record Board Assembly Drawing	0285-0260
Sweep and Record Board List of Materials	0285-0260

ADC Board

ADC Board Schematic	0285-0341
ADC Board Assembly Drawing	0285-0340
ADC Board List of Materials	0285-0340

Attenuator Board

Attenuator Board Schematic	0285-0301
Attenuator Board Assembly Drawing	0285-0300
Attenuator Board List of Materials	0285-0300

Interface Option Board

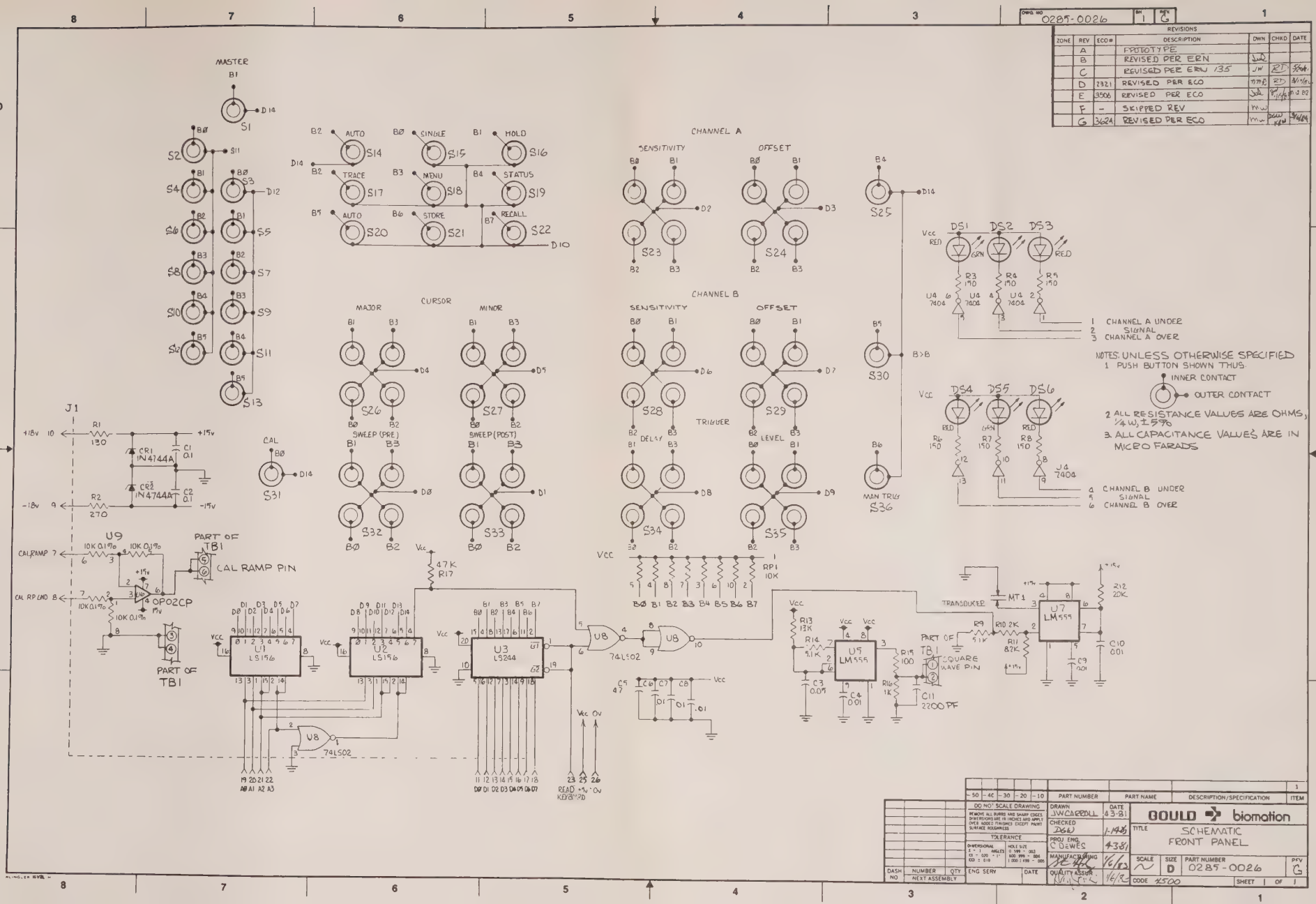
Interface Board Schematic	0285-0061
Interface Board Assembly Drawing	0285-0060
Interface Board List of Materials	0285-0060

Floppy Disk

Floppy Controller Board Schematic	0285-0056
Floppy Controller Board Assembly Drawing	0285-0055
Floppy Controller Board List of Materials	0285-0055
Floppy Disk, Top Assembly Drawing	0285-0296
Floppy Disk, Top Assembly List of Materials	0285-0296

Power Supply

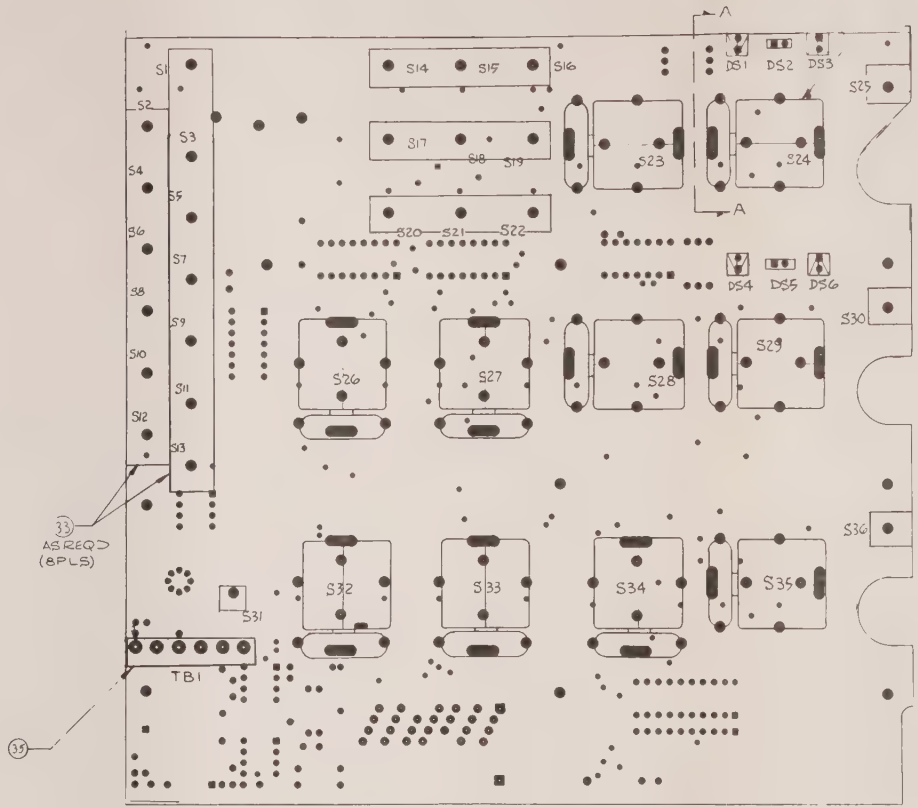
Power Supply Top Assembly Drawing	0285-0003
Power Supply Top Assembly List of Materials	0285-0003
Heatsink Assembly Drawing	0285-0173
Heatsink Assembly List of Materials	0285-0173
Faceplate Assembly Drawing	0285-0156
Faceplate Assembly List of Materials	0285-0156
Filter Board List of Materials	0285-0180
Filter Board Schematic	0285-0181
Filter Board Assembly Drawing	0285-0180
Power Supply Board Schematic	0285-0011
Power Supply Board Assembly Drawing	0285-0010
Power Supply Board List of Materials	0285-0010



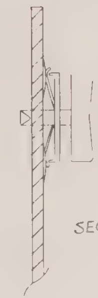
DWG NO 0285-0026
SH 1
REV G
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
A PROTOTYPE
B REVISED PER ERN
C REVISED PER ERN 135
D 2321 REVISED PER ECO
E 3506 REVISED PER ECO
F - SKIPPED REV
G 3624 REVISED PER ECO
MASTER
CHANNEL A
SENSITIVITY
OFFSET
CHANNEL B
CURSOR
MAJOR
MINOR
SWEEP (PRE)
SWEEP (POST)
TRIGGER
DELAY
LEVEL
CAL
MAN TRIG
1 CHANNEL A UNDER
2 SIGNAL
3 CHANNEL A OVER
4 CHANNEL B UNDER
5 SIGNAL
6 CHANNEL B OVER
NOTES: UNLESS OTHERWISE SPECIFIED
1. PUSH BUTTON SHOWN THUS.
INNER CONTACT
OUTER CONTACT
2. ALL RESISTANCE VALUES ARE OHMS, 1/4 W, ±5%
3. ALL CAPACITANCE VALUES ARE IN MICRO FARADS
CAL RAMP PIN
PART OF TB1
SQUARE WAVE PIN
TRANSDUCER
U1 LS156
U2 LS156
U3 LS244
U5 LM555
U7 LM555
U8 74LS02
U9 OP02CP
J1
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DRAWN JWCARROLL DATE 4-3-81
CHECKED DGW 1-14-83
PROJ ENG. C DEWES 4-3-81
MANUFACTURING 1/6/83
QUALITY ASSUR. 1/6/83
GOULD biomation
TITLE SCHEMATIC FRONT PANEL
SCALE
SIZE D
PART NUMBER 0285-0026
REV G
CODE 4500
SHEET 1 OF 1
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM

DWG NO 0285-0025 SH 1 REV G

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PROTO TYPE	JWC		11580
	B		REVISED PER ERN			
	C		P...O RUN PER ERN 135	RW	RD	5-1-8
	D	2026	REVISED PER ECO	MS	RG	[illegible]
	E	2321	REVISED PER ECO	mmB	RD	3/9/81
	F	3506	REVISED PER ECO NO	[illegible]	[illegible]	[illegible]
	F		PROD. REL PER ERN #262	DGW	4/14/82	
	G	3626A	REVISED PER ECC	M.W		



SOLDER SIDE



SECTION A-A

NOTES: UNLESS OTHERWISE SPECIFIED
1. DS1-6 : LONG LEAD (CATHODE) TO BE INSTALLED IN SQUARE PAD HOLE.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO	NUMBER (NEXT ASSEMBLY)	QTY
-1	0285-105	1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY AFTER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL		HOLE SIZE	
X = 1	ANGLES	0 .599	.003
.XX = .020	± 1°	.600 .999	.004
.XXX = .010		1.000 1.499	.005

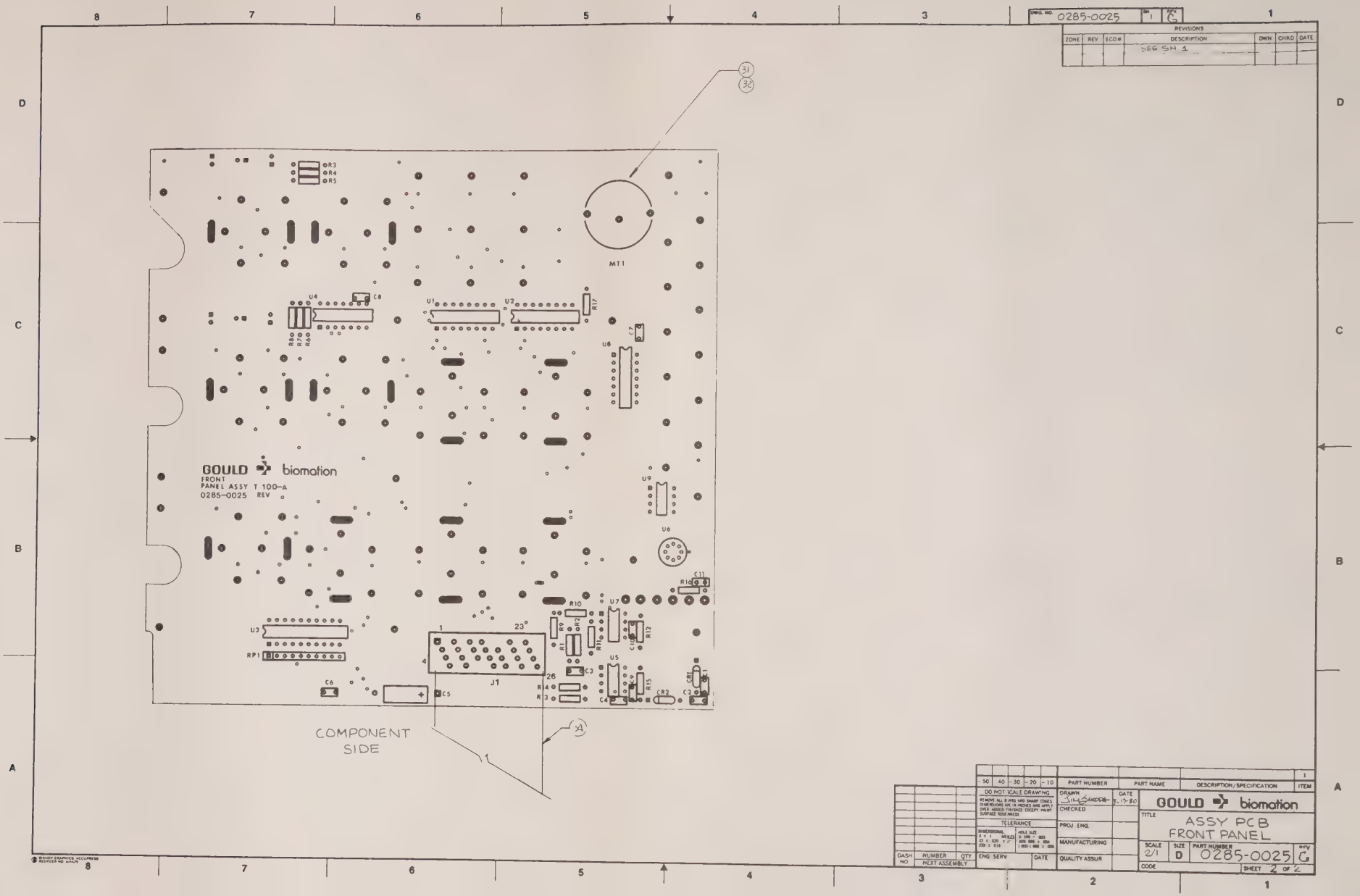
		DATE
DRAWN	JWCARROLL	11-5-80
CHECKED	DGW	1-14-83
PROJ ENG	DRJ	1-6-83
MANUFACTURING	[illegible]	1/6/83
QUALITY ASSUR	[illegible]	[illegible]
ENG SERV		

GOULD biomation

TITLE: ASSY, PCB FRONT PANEL

SCALE 2/1 | SIZE D | PART NUMBER 0285-0025 | REV G

CODE 4500 | SHEET 1 OF 2



DWG. NO. 0285-0025
SH 1
REV G
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
SEE SH 1
31
32
R3
R4
R5
MT1
U4
C8
U1
U2
R17
R8
R7
R6
C7
U8
GOULD biomation
FRONT
PANEL ASSY T 100-A
0285-0025 REV
U9
U6
C11
R16
R10
U7
U3
RP1
1
23
R9
R1
R11
C10
R12
4
J1
26
C3
U5
C6
C5
R4
R3
C4
R15
CR2
CR1
C1
C2
COMPONENT
SIDE
A
-50
40
-30
-20
-10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
1
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DRAWN
DATE
5-13-80
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
ASSY PCB
FRONT PANEL
SCALE
2/1
SIZE
D
PART NUMBER
0285-0025
REV
G
CODE
SHEET 2 OF 2

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING
	RES .4

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0285-0027	FABRICATION			FRONT PANEL	
2						10	0285-0111	SWITCH ASSY	S23,24,26-29 32-35			
3												
4						1	1800-0005	IC	U4	7404		
5						1	1800-0240	IC	U3	74LS244		
6						2	1800-0301	IC	U1,2	74LS156		
7						2	1700-0078	IC	U5, U7	LM 555		
8						1	1700-0103	IC	U6	OP02CJ		
9						1	1800-0106	IC	U8	74LS02		
10						1	3700-0079	IC	U9	10K 8 PIN DIP	RESISTOR PAK	
11						2	1100-0027	DIODE	CR1,2	IN4744A	ZENER	
12						4	6400-0056	LED	DS1,3,4,6		RED TRIANGLE	
13						2	6400-0055	LED	DS2,5		GREEN BAR	
14						1	4010-0222	CAPACITOR	C11	2200PF		
15						2	4010-0104	CAPACITOR	C1,2	0.1 uf		
16						6	4010-0103	CAPACITOR	C4,6,7-10	.01 uf		
17						1	4300-0002	CAPACITOR	C5	4.7uf		
18						1	4010-0563	CAPACITOR	C3	.056 uf		

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE				
B	REVISED PER ERN				
C	PILOT RUN PER ERN 135	5/11/81			
D	REVISED PER ECO 2026	10-1-81			
E	REVISED PER ECO 2321	3-3-82			
F	REVISED PER ECO NO 3506	1-4-88			
F	PROD REL PER ERN Nº 262	12-6-84	DGW		

DRAWN	JIM SAKODA	DATE	5-9-80
CHECKED	DGW		1-10-83
ENGINEER	DRJ		1-6-83
MANUFACTURING			1/6/83
QUALITY ASSURANCE			1-7-83

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL
FRONT PANEL
P.C.B.

biomation

B | 0285-0025 | REV G

MODEL 4500 | CODE | SHEET 1 OF 2

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19						1	3000-1000	RESISTOR	R15		100Ω, 1/4W, 5%	
20						6	3000-1500		R3-8		150Ω, 1/4W, 5%	
21						1	3000-1300		R1		130Ω, 1/4W, 5%	
22						1	3000-1001		R16		1KΩ, 1/4W, 5%	
23						2	3000-5101		R9,14		5.1KΩ, 1/4W, 5%	
24						1	3000-2001		R10		2KΩ, 1/4W, 5%	
25						1	3000-1302		R13		13KΩ, 1/4W, 5%	
26						1	3000-8201		R11		8.2K, 1/4W, 5%	
27						1	3000-2002		R12		20K, 1/4W, 5%	
28						1	3000-4701	RESISTOR	R17		4.7K, 1/4W, 5%	
29						1	3000-2700	RESISTOR	R2		270Ω, 1/4W, 5%	
30						1	3700-0066	RES PACK	RP1		10K, 10 PIN SIP	
31						1	7400-0001	TRANSDUCER	MT1			
32						1	7000-0428	XDUCER, MTG				
33						AR		FOAM TAPE				
34						1	0285-0123	CABLE ASSY ENT PNL				LM
35						1	0285-0121	TEST PT ASSY				
36												

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
G	REVISED PER ECO 3624	8/13	MW		

DRAWN		DATE	
CHECKED			
ENGINEER			
MANUFACTURING			
QUALITY ASSURANCE			

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL
FRONT PANEL
P.C.B.

biomation

B | 0285-0025 | REV G

MODEL 4500 | CODE | SHEET 2 OF 2

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0285-0025	FNT PNL RB				LM
2						1	0285-0118	BEZEL				
3						1	0285-0107	FNT PNL				
4						20	0285-0110-02	PB CAPS			DK GREY	
5						6	0285-0110-01	" "			LT GREY	
6						1	0119-0030	EXTRUSION FNT PNL				
7						12	7000-0160	SPACERS			#6 x 1/4" LONG	
8												
9						1	0285-0130	CRT PCB				LM
10						2	7000-0141	STAND OFF			#6 x 3/4" LONG	
11						1	0285-0348	CABLE ASSY				
12												
13												
14												
15												
16												
17												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL PER ERN 135	4-24-81	ORS	RD	
B	REVISED PER ECO NR 2337	3-13-81	JW	KW	
C	REV. PER ECO #2697	3-16-82	MW	DKW	
C	PROD REL PER ERN #262	12-16-82	DKW	DKW	2-14-83
D	REV'D PER ECO	11-15-88	SAR	DKW 11-17-88	DKW

DASH NO	NUMBER	QTY
-10	0285-0102	1

NEXT ASSEMBLY

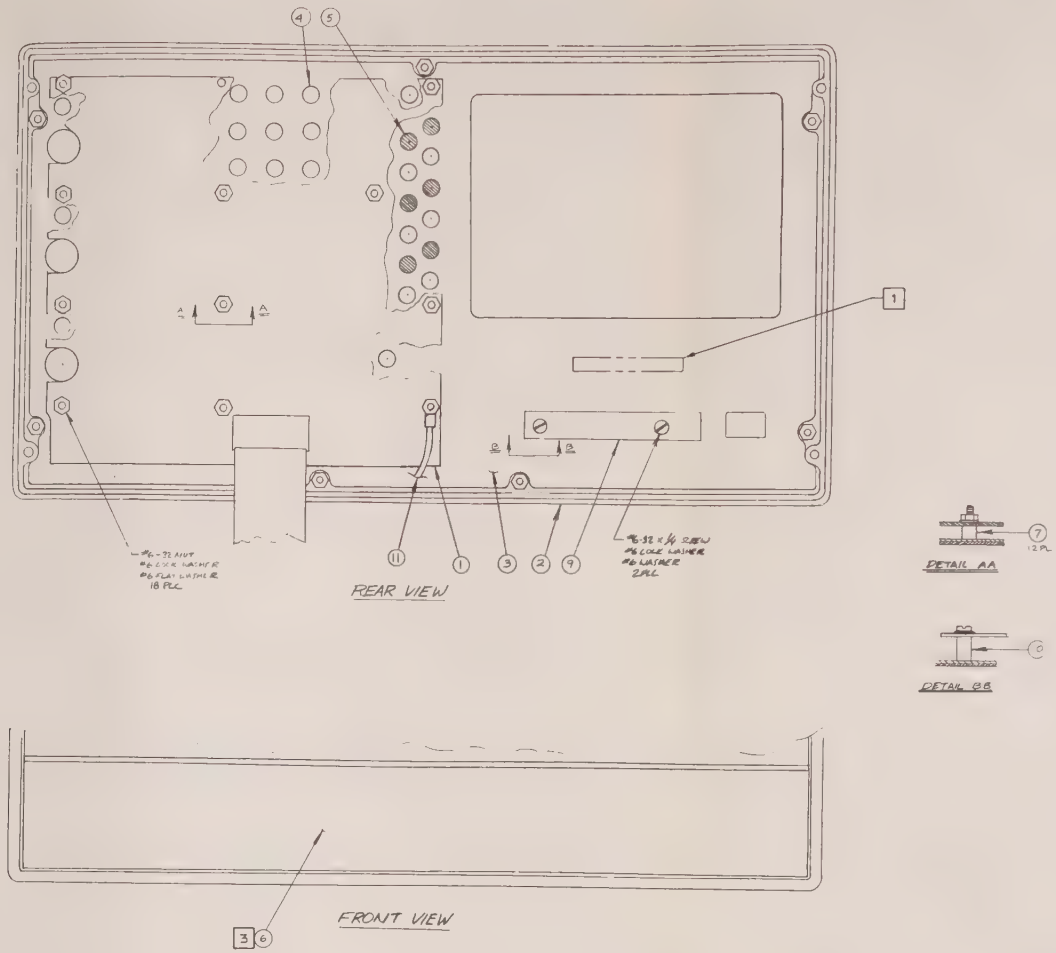
	DATE
DRAWN SANDELL	2 9 81
CHECKED DKW	1-10-83
ENGINEER DRS	1-6-83
MANUFACTURING	1/6/83
QUALITY ASSURANCE	1/7/83

LIST OF MATERIAL
BEZEL ASSY

biomation

B | 0285-0105 | REV D

MODEL 4500 | CODE | SHEET 1 OF 1



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK ASSY NO., DASH NO., REVISION LEVEL, SERIAL NO., AND VENDOR LOGO APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK OR APPROVED LABEL.
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.
3. CLEAN MATING SURFACE WITH A DAMP CLOTH (WATER) PRIOR TO SECURING EXTRUSION.

DWG. NO 0285-0105 SH 1 REV D

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL PER ERN 135	DRS	RD	5/1/81
	B	2381	REVISED PER ECO #	DRS	DLW	3-15-82
	C	2697	REVISED PER ECO	MW	DLW	[illegible]
	C		PROD REL PER ERN #262	DLW	DLW	2-4-83
	D	4077	REV'D PER ECO	SAR	DOW DRS	11/17/83

-10	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 UNLESS .XX ± .030 ± 1° .XXX ± .010

HOLE SIZE: 0 .999 ± .002 .000 .999 ± .004 1.000 1.999 ± .005

ENG. SERV. | DATE

DRAWN SANDELL DATE 2 9 81

CHECKED DLW 1-14-83

PROJ ENG. DRS 1-6-83

MANUFACTURING [signature] 1/6/83

QUALITY ASSUR [signature] 1/6/83

GOULD biomation

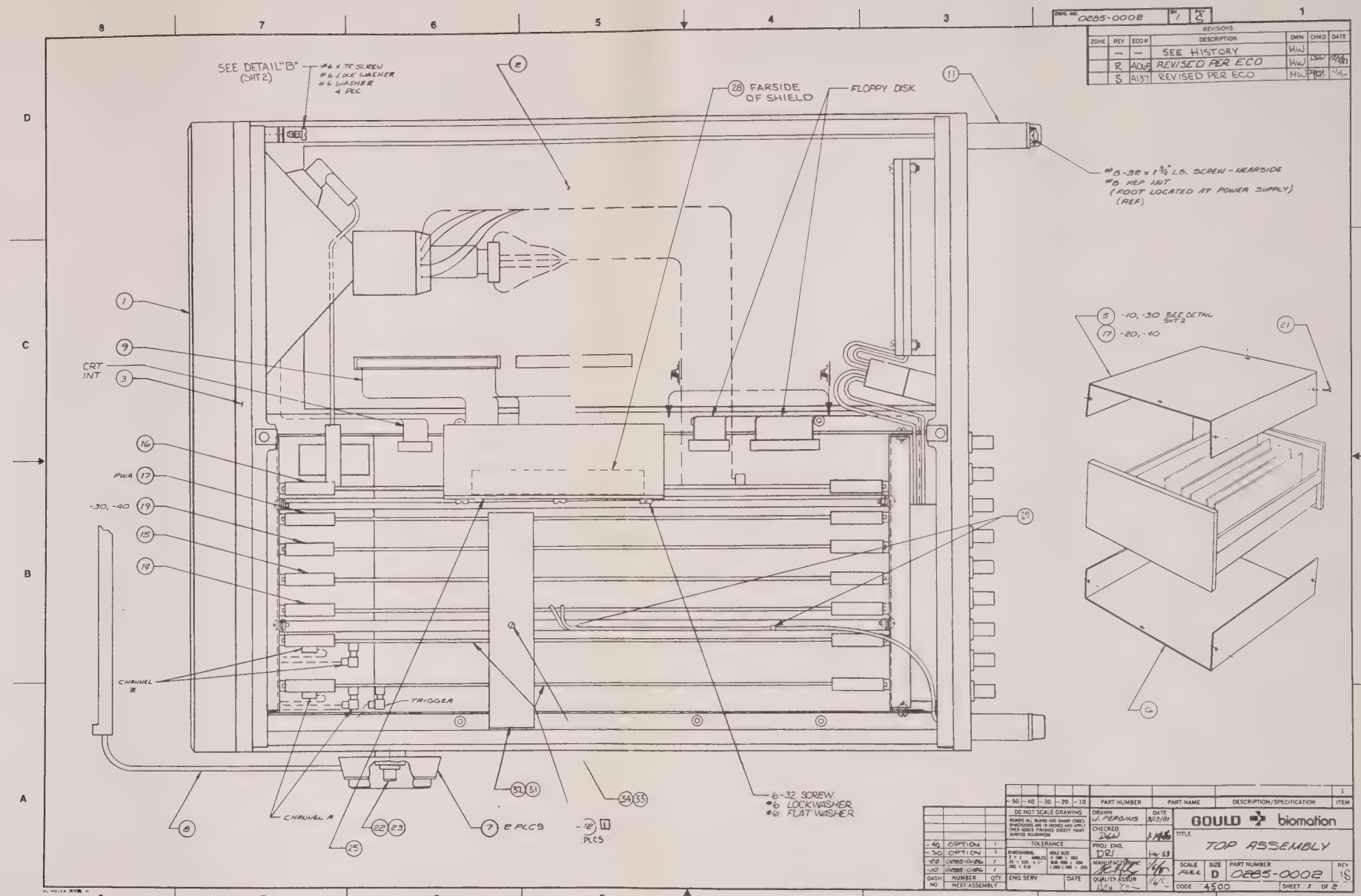
TITLE BEZEL ASSY

SCALE FULL | SIZE D | PART NUMBER 0285-0105 | REV D

CODE 4500 | SHEET 1 OF 1

DASH NO	NUMBER	QTY
-10	0286-0002	1

NEXT ASSEMBLY

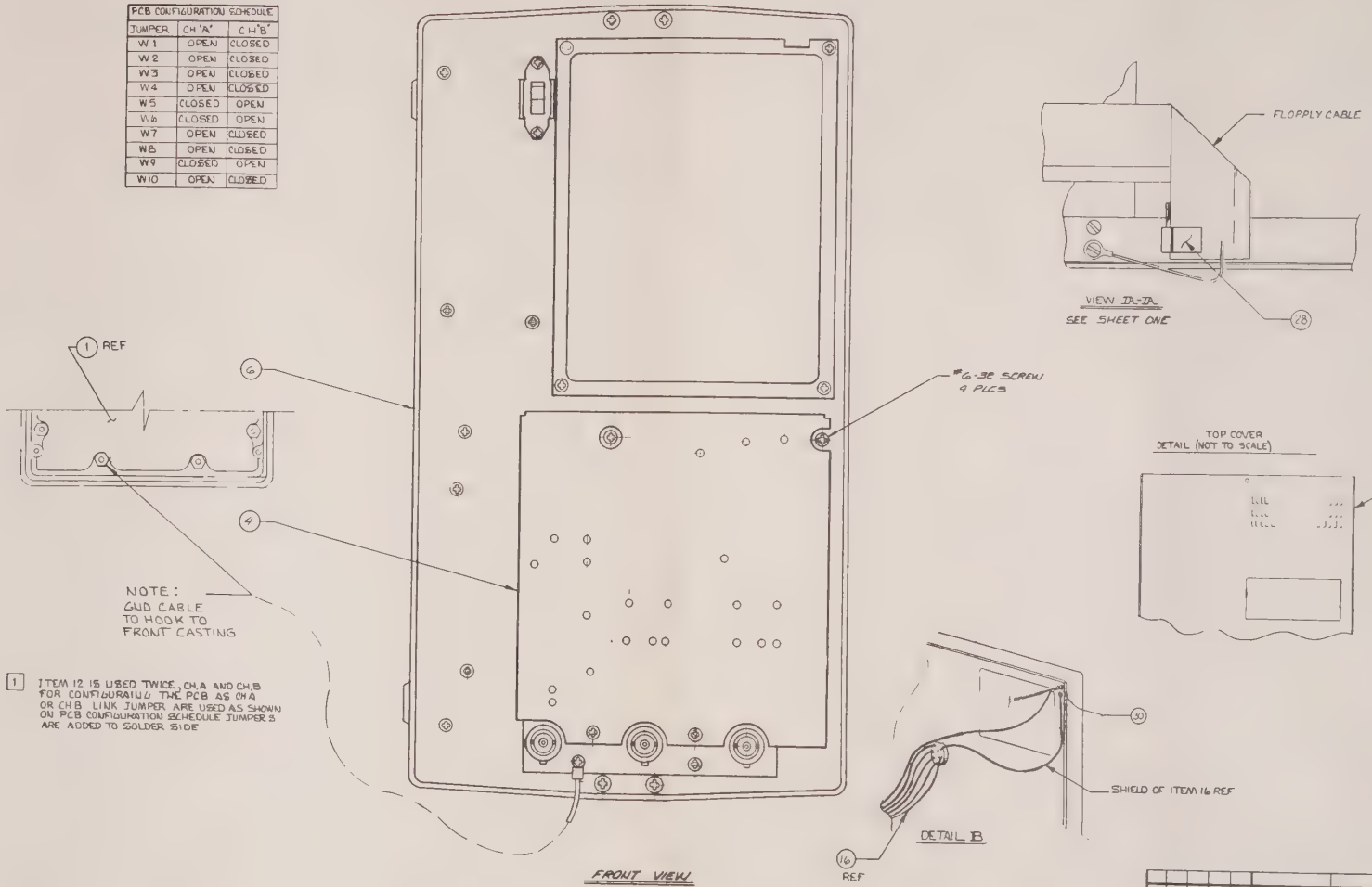


DWG. NO. 0285-0002
SH 1
REV S
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
— | — | — | SEE HISTORY | MW
R | 4045 | REVISED PER ECO | MW
S | 4137 | REVISED PER ECO | MW
SEE DETAIL "B" (SHT 2)
#6 x .75 SCREW
#6 LOCK WASHER
#6 WASHER
4 PLC
28 FARSIDE OF SHIELD
FLOPPY DISK
#8-32 x 1 3/4" LG. SCREW - NEARSIDE
#8 KEP NUT
(FOOT LOCATED AT POWER SUPPLY)
(REF)
5 -10, -30 SEE DETAIL SHT 2
17 -20, -40
CRT INT
PWA
-30, -40
CHANNEL
TRIGGER
CHANNEL A
7 2 PLCS
-12 1 PLCS
6-32 SCREW
#6 LOCKWASHER
#6 FLAT WASHER
-50 -40 -30 -20 -10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
DRAWN J. PERGINS
DATE 3/13/81
CHECKED DGW
PROJ ENG. DRI
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
TOLERANCE
-40 OPTION 1
-30 OPTION 1
-20 0285-0126 1
-10 0285-0126 1
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE TOP ASSEMBLY
SCALE FULL
SIZE D
PART NUMBER 0285-0002
REV 18
CODE 4500
SHEET 1 OF 2

DWG NO.	SH	REV
0285-0002	2	S

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			

PCB CONFIGURATION SCHEDULE		
JUMPER	CH 'A'	CH 'B'
W1	OPEN	CLOSED
W2	OPEN	CLOSED
W3	OPEN	CLOSED
W4	OPEN	CLOSED
W5	CLOSED	OPEN
W6	CLOSED	OPEN
W7	OPEN	CLOSED
W8	OPEN	CLOSED
W9	CLOSED	OPEN
W10	OPEN	CLOSED



[1] ITEM 12 IS USED TWICE, CH.A AND CH.B FOR CONFIGURAING THE PCB AS CH.A OR CH.B. LINK JUMPER ARE USED AS SHOWN ON PCB CONFIGURATION SCHEDULE JUMPERS ARE ADDED TO SOLDER SIDE

DASH NO	NUMBER	QTY	NEXT ASSEMBLY
			ENG SERV DATE

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DO NOT SCALE DRAWING

TOLERANCE

DRAWN	C. PERKINS	DATE 3/17/81
CHECKED	JKN	
PROJ ENG		
MANUFACTURING		
QUALITY ASSUR		

GOULD biomation

TITLE: TOP ASSEMBLY

SCALE	SIZE	PART NUMBER	REV
FULL	D	0285-0002	S

CODE 14500 SHEET 2 OF 2

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1			1	1	1	1	0285-0105	BEZEL ASSY				LM
2			1	1	1	1	0285-0003	POWER SUPPLY ASSY				LM
3			1	1	1	1	0285-0019	CHASSIS ASSY				LM
4			1	1	1	1	0285-0154	ATTENUATOR ASSY				LM
5			—	1	—	1	0114-0039-10	COVER, TOP				
6			1	1	1	1	0114-0039-20	COVER, BOTTOM				
7			2	2	2	2	0111-0059	BAIL, KNOB				
8			1	1	1	1	0111-0016	HANDLE ASSY				LM
9												
10												
11			1	1	1	1	0950-0099	FOOT				
12			2	2	2	2	0285-0340-10	CHI ADC, PWA				LM
13												LM
14			1	1	1	1	0285-0260	SWEEP REC, PWA				LM
15			1	1	1	1	0285-0045	CONTROLLER, PWA				LM
16			1	1	1	1	0285-0050	CRT DRIVER, PWA				LM
17			1	—	1	—	0285-0055-10	PWA FLOPPY				LM
18												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	—	SEE HISTORY				
	Q	REVISED PER ECO 3735	10/28/82	JWC	DGW	KJZ
	R	REVISED PER ECO 4065	1/28/83	MW	DGW	
	S	REVISED PER ECO 4137	4/26/83	MW	DGW	DRS

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-40	OPTION	1
-30	OPTION	1
-20	0285-0126	1
-10	0285-0126	1

	DRAWN	DATE
	J. PERGINS	3/9/82
	CHECKED DGW	1-10-83
	ENGINEER DRS	1-6-83
	MANUFACTURING	1/6/83
	QUALITY ASSURANCE	1/6/83

LIST OF MATERIAL

TOP ASSEMBLY

MODEL 4500

biomation

B | 0285-0002 | REV S

CODE | SHEET 1 OF 2

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19			1	1	—	—	0285-0060	INTERFACE PWB OPTION				LM
20												
21			12	12	12	12	7000-0368	SCREW			#6-32 x 3/8" LG 100° FLAT HEAD	
22			2	2	2	2	7000-0376	SCREW, SOC HD CAP			1/4"-20 x 3/4" LG	
23			2	2	2	2	—	WASHER			1/4" SPLIT LOCK, HEL	
24												
25			1	1	1	1	0285-0317	SHIELD				
26												
27												
28			1	1	1	1	7000-0401	FOAM TAPE			1/8 x 1 x 4"	
29			2	2	2	2	7200-0008	CABLE TIE				
30			1	1	1	1	7000-0577-10	LUG, SLIP ON, MALE				
31			1	1	1	1	0451-0073-01	RETAINER				
32			1	1	1	1	0451-0072-01	BRACKET				
33			1	1	1	1	7011-1440-20	SCREW			#4 PAN HEAD	
34			1	1	1	1	7083-1004-00	WASHER			#4 LOCK	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

	DRAWN	DATE
	J. PERGINS	3/9/82
	CHECKED	
	ENGINEER	
	MANUFACTURING	1/6/83
	QUALITY ASSURANCE	

LIST OF MATERIAL

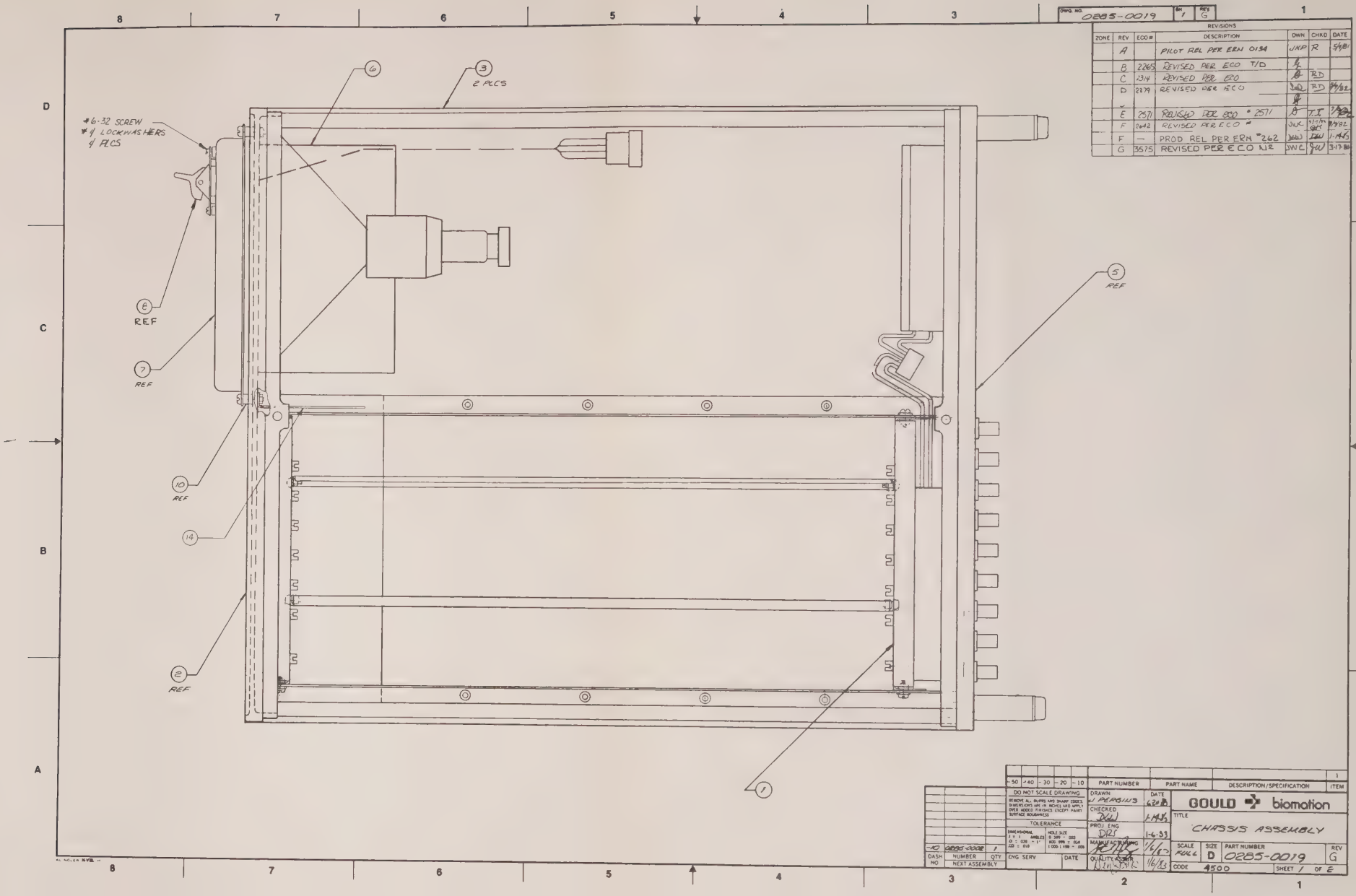
TOP ASSEMBLY

MODEL 4500

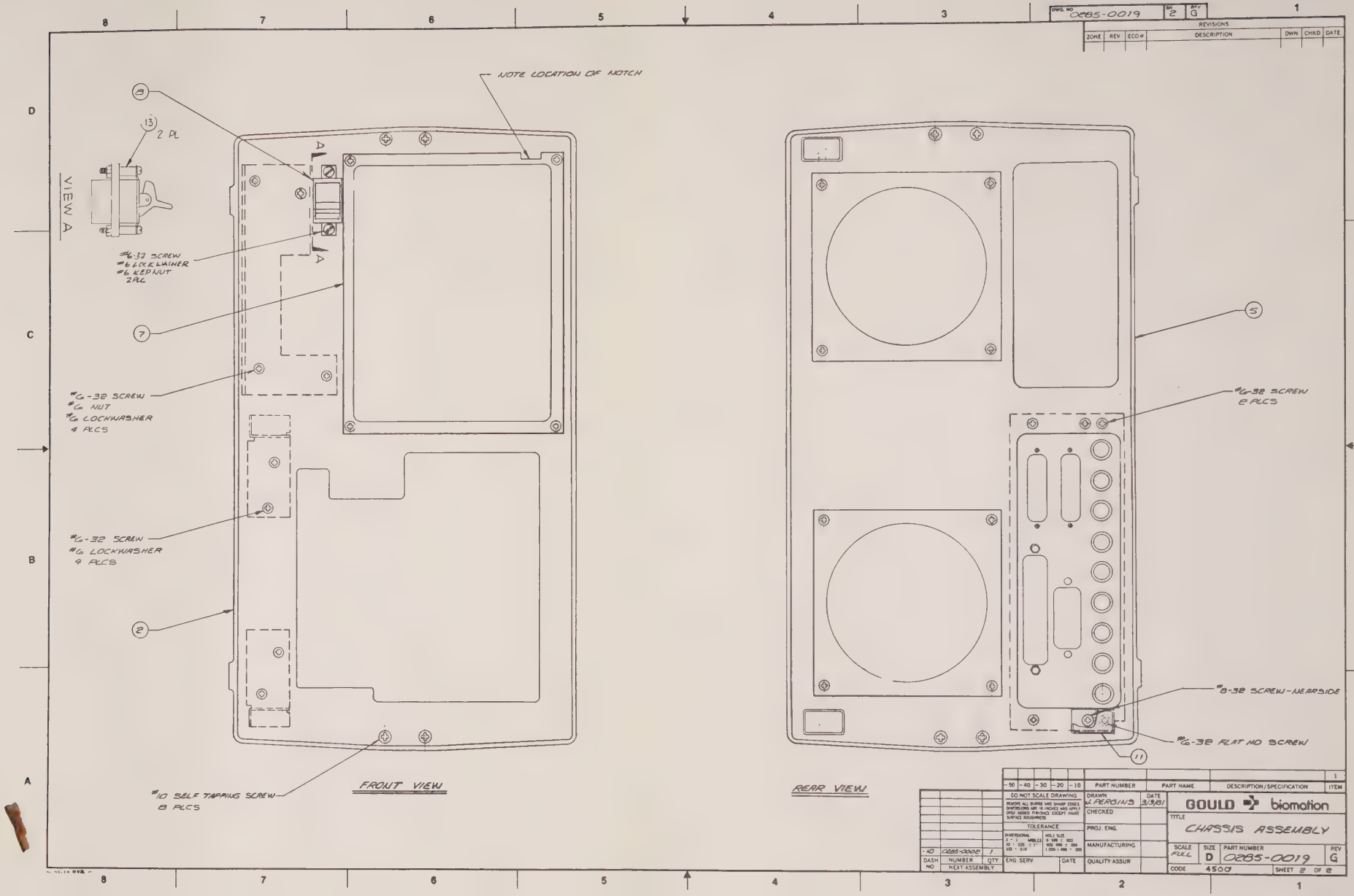
biomation

B | 0285-0002 | REV S

CODE | SHEET 2 OF 2



DWG. NO. 0285-0019
SH 1
REV G
REVISIONS
ZONE | REV | ECO # | DESCRIPTION | DWN | CHKD | DATE
A | PILOT REL PER ERN 0134 | JKP | R | 5/4/81
B | 2265 | REVISED PER ECO T/D
C | 2314 | REVISED PER ECO
D | 2279 | REVISED PER ECO
E | 2571 | REVISED PER ECO # 2571
F | 2642 | REVISED PER ECO #
F | — | PROD REL PER ERN #262
G | 3575 | REVISED PER ECO N2
#6-32 SCREW
#4 LOCKWASHERS
4 PLCS
6
3
2 PLCS
8
REF
7
REF
10
REF
14
2
REF
5
REF
1
-50 -40 -30 -20 -10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL
HOLE SIZE
DRAWN J PERGINS
DATE 6-20-83
CHECKED DWJ
1-14-83
PROJ ENG DRS
1-6-83
MANUFACTURING
1/6/83
QUALITY ASSUR
1/6/83
GOULD biomation
TITLE CHASSIS ASSEMBLY
SCALE FULL
SIZE D
PART NUMBER 0285-0019
REV G
CODE 4500
SHEET 1 OF 2
-10 0285-0002 1
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE



DWG. NO 0285-0019
SH 2
REV G
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
NOTE LOCATION OF NOTCH
VIEW A
13
2 PL
#6-32 SCREW
#6 LOCKWASHER
#6 KEP NUT
2 PLC
#6-32 SCREW
#6 NUT
#6 LOCKWASHER
4 PLCS
#6-32 SCREW
#6 LOCKWASHER
4 PLCS
#10 SELF TAPPING SCREW
8 PLCS
FRONT VIEW
REAR VIEW
#6-32 SCREW
2 PLCS
#8-32 SCREW-NEARSIDE
#6-32 FLAT HD SCREW
-50
-40
-30
-20
-10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
DRAWN
J. PERSINS
DATE
3/3/81
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
TOLERANCE
ENG SERV
DATE
GOULD biomation
TITLE
CHASSIS ASSEMBLY
SCALE
FULL
SIZE
D
PART NUMBER
0285-0019
REV
G
CODE
4500
SHEET 2 OF 2
-10
0285-0002
1
DASH NO
NUMBER
QTY
NEXT ASSEMBLY

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0285-0217	CARD CAGE ASSY				LM
2						1	0114-0041	FRONT CASING				
3						2	0285-0117	EXTRUSION SIDE RAIL				
4												
5						1	0285-0214	REAR CASTING ASSY				LM
6						1	0950-0163	POWER SUPPLY BRACKET				
7						1	0950-0131-20	CRT ASSY			GRN	LM
8						1	0285-0218	CABLE ASSY-POWER SWITCH				LM
9												
10						4	7000-0434	SPACER				
11						1	0950-0099	FOOT				
12												
13						2	7000-0440	SPACER	——		5/10 LG. CL #6	
14						1	0285-0321	SHIELD CRT				

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL PER ERN 0134	3/9/81	JKP	R	
B	REVISED PER ECO NO 3575	3/7/83	SWC	DW	
C	REVISED PER ECO # 2314			RD	
D	REVISED PER ECO # 2379	7-9-82		RD	
E	" " " # 2571	5-21-82			
F	" " " # 2642	6-24-82		T.J.	
G	PROD REL PER ERN #262	DW	DW	1-4-83	

DASH NO	NUMBER	QTY
-10	0285-0002	1
	NEXT ASSEMBLY	

	DRAWN	DATE
	J. PERGINS	3/9/81
	CHECKED DW	1-4-83
	ENGINEER DW	1-6-83
	MANUFACTURING	1/6/83
	QUALITY ASSURANCE	1/6/83

LIST OF MATERIAL

CHASSIS ASSEMBLY

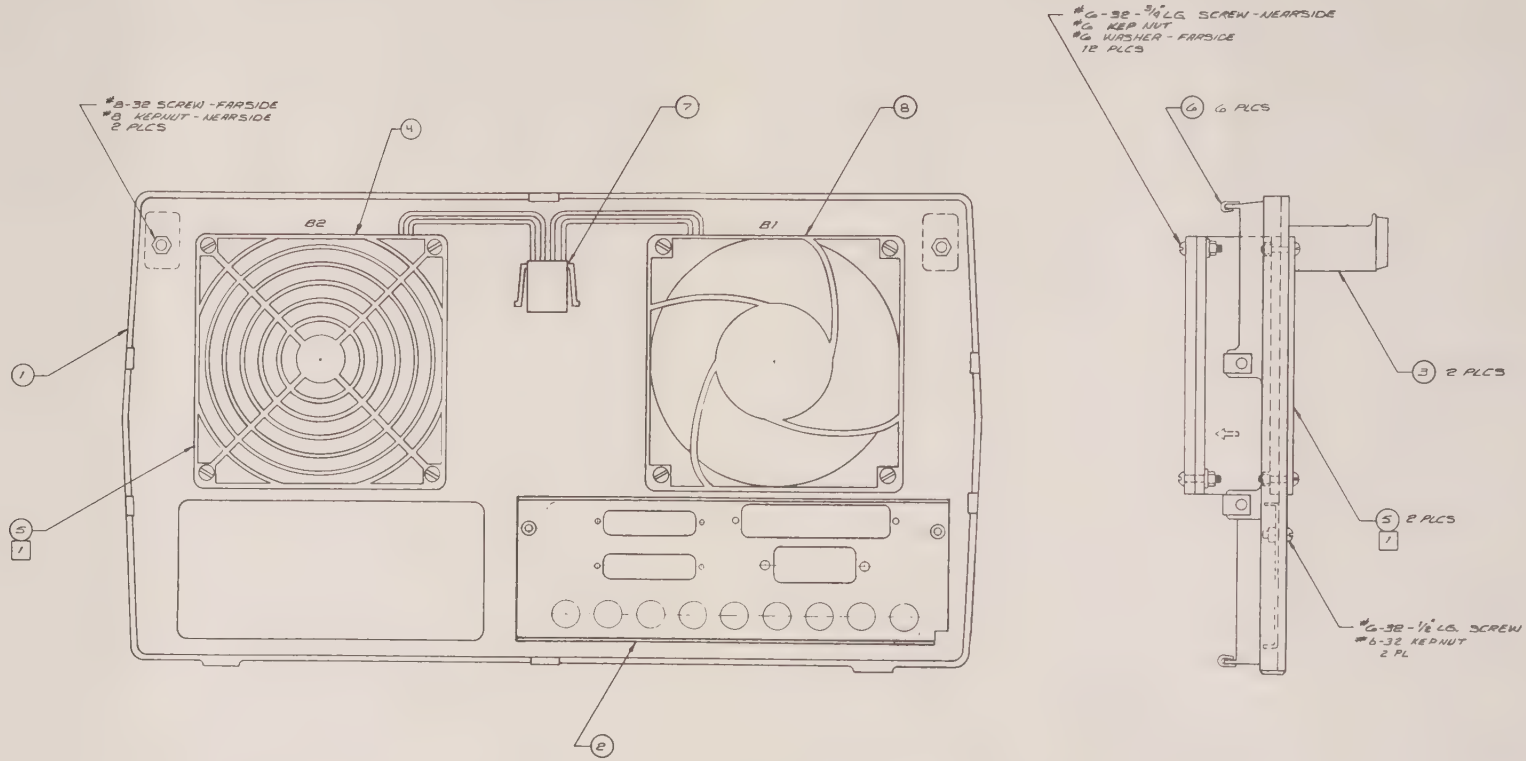
biomation

B 0285-0019 REV G

MODEL 4500 | CODE | SHEET 1 OF 1

DWG. NO 0285-0214 SH 1 REV C

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL PER EBN 0134	JKP	RG	5/11/83
	B	2289	REVISED PER ECO#	JWC	RG	1-4-83
	C	2314	REVISED PER ECO# PROD. REL PER ERN #262	[illegible]	RD	



NOTE

1 ITEM 5 (FAN GUARD) MUST BE PLASTIC VERSION.

WIRING INSTRUCTIONS		
TO	FROM	COLOR
P3-1	B1-A	BLU/BLK
P3-2	B1-B	WHT/BRN
P3-3	B2-A	BLU/BLK
P3-4	B2-B	WHT/BRN

DASH NO	NUMBER	QTY
-10	0285-0019	1
	NEXT ASSEMBLY	

-50	40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES; .XX ± .020 ± 1°; .XXX ± .010

HOLE SIZE: .0 .999 ± .003; .000 .999 ± .004; 1.000-1.999 ± .005

ENG SERV | DATE

		DATE
DRAWN	J. PERGIUS	2/23/81
CHECKED	DW	1-14-83
PROJ ENG.	DRS	1-6-83
MANUFACTURING	[illegible]	1/6/83
QUALITY ASSUR	[illegible]	1/6/83

GOULD biomation

TITLE: ASSEMBLY - REAR CASTING

SCALE	SIZE	PART NUMBER	REV
	D	0285-0214	C

CODE 4500 SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0285-0009	REAR CASTING				
2						1	0285-0308	INTERFACE PNL ASSY				
3						2	0950-0099	FOOT				
4						1	2900-0002	FAN	B2			
5						3	7000-0080	GUARD, FAN				
6						6	7000-0334	MTG. NUT				
7						1	0285-0215	CABLE ASSY-FAN				LM
8						1	2900-0003	FAN	B1			

ASSEMBLY TIME | COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL PER ERN C134	3/9/81	JKP	RG	
B	REVISED PER ECO No 2289	6-16-81	JWC	RG	
C	REVISED PER ECO No 2314			ZD	
C	PROD REL PER ERN # 262	6-1-82		DGW	

DASH NO.	NUMBER	QTY
-10	0285-0019	1

NEXT ASSEMBLY

	DATE
DRAWN J. PERGINS	2/20/81
CHECKED DGW	1-10-83
ENGINEER DRS	1-6-83
MANUFACTURING	1/6/83
QUALITY ASSURANCE	1/6/83

LIST OF MATERIAL

ASSEMBLY-
REAR CASTING

biomation

B 0285-0214 REV C

MODEL 4500 CODE SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY 60	-50	-40	30	20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1			—	—	—	1	9000-0029-10	CRT	WHITE	C822P4	NIPPON ELECT. WHITE	
2			1	1	1	—	9000-0029-30	CRT	GREEN	C822P4	NIPPON ELECT GREEN	
3			1	—	—	1	9000-0047-20	DEFLECTION COIL				
4			—	—	1	—	9000-0047-30	DEFLECTION COIL				
5			—	1	—	—	9000-0047-10	DEFLECTION COIL				
6			A/R	A/R	A/R	A/R	7100-0067	BRAID		2162	ALPHA 1/16 O.D. APPROX 7 IN.	
7			1	1	1	1	7000-0375	SPRING				
8			2	2	2	2	———	GND LUG			#6	
9												
10												
11												
12												
13												
14			A/R	A/R	A/R	A/R	2000-0006	MAGNET PINCUSHION				
15												
16												
17												
18												

ASSEMBLY TIME | COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTO TYPE	3-21-80	JWC		
G	REVISED PER ECO # 3588	6-8-80	JWC	DGW	6-17-82
C	PROD REL ERN #127	4-9-81	MB		
D	REVISED PER ECO # 1735	5-22-81	JWC		
E	REVISED PER ECO # 2278	6-28-82	JWC	ZD	
F	REV'D PER ECO # 2447	7/29/82			

DASH NO	NUMBER	QTY
-30	0112-0200	1
-40	0114-1003	1
-20	0285-0019	1
-40	0114-0003	1
-40	0950-0003	1

NEXT ASSEMBLY

	DATE
DRAWN N. Cassetti	3-22-80
CHECKED R. Dean	4/13/81
ENGINEER	4/10/81
MANUFACTURING	4/10/81
QUALITY ASSURANCE	4-10-81
R. Gipson	4/10/81

LIST OF MATERIAL

CRT ASSEMBLY

biomation

B 0950-0131 REV G

MODEL ALL CODE SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0111-0058	HANDLE, ADJUSTABLE				
2						2	9000-0028	SPRING COMPRESSION				
3						2	0111-0018	SPROCKET, HANDLE				
4						2	0111-0019	HUB HANDLE				
5						1	0117-0204-10	LABEL, HANDLE				

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
—	RELEASED TO PRODUCTION EN 0902	9/26/78	RG		
A	REVISED PER ECO No 6885	9/17/79	JC	[illegible]	
B	REVISED PER ECO # 1764	6-26-8	JWD	[illegible]	7-24-81
C	REVISED PER ECO 3848	7/11/83	mw	[illegible]	7-12-8

DASH NO.	NUMBER	QTY
-10	0111-0001-20	1
-10	0320-0001	1
-10	0112-0003	1

NEXT ASSEMBLY

		DATE
DRAWN	R.G.	9/25/78
CHECKED	[illegible]	9-26-78
ENGINEER		
MANUFACTURING	[illegible]	10/12/78
QUALITY ASSURANCE	[illegible]	10/13/78

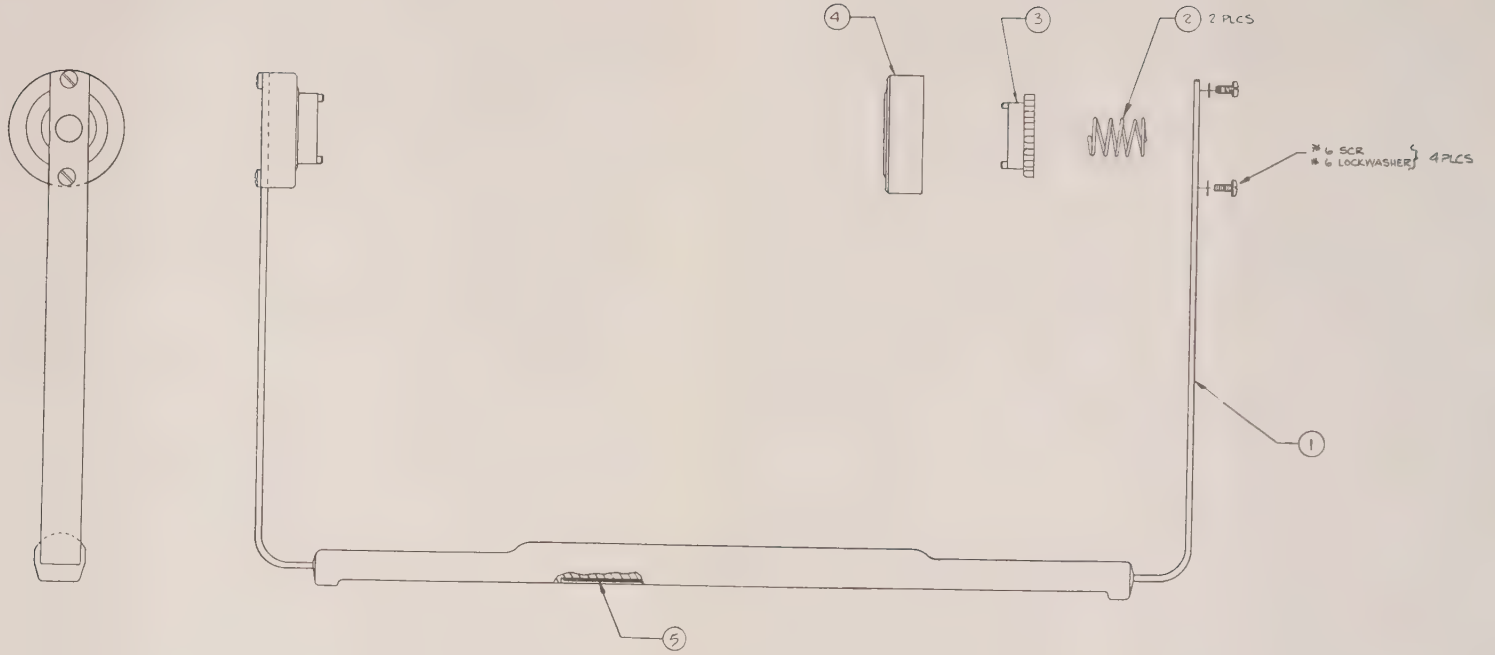
LIST OF MATERIAL
ASSY, HANDLE

biomation

B 0111-0016 REV C

MODEL K100-D CODE SHEET 1 OF 1

REV —: RELEASED TO PRODUCTION
EN 0902 RG 9/26/78
REV A: REVISED PER ECO #0885 [illegible]
REV B: REVISED PER ECO #1764 [illegible]
B: PROD. REL PER ERN #2626 [illegible]
C: REVISED PER ECO 3848 [illegible]

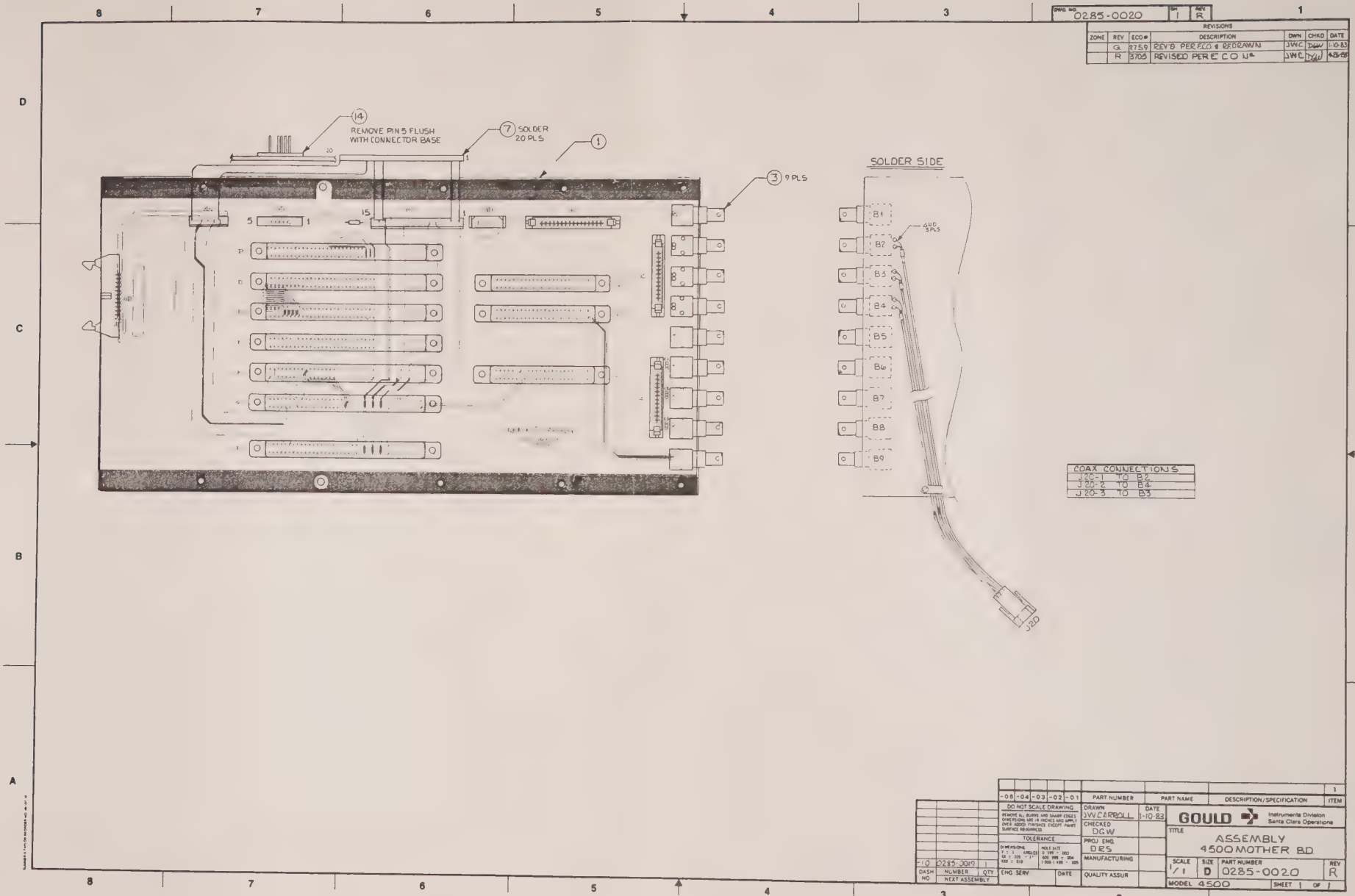


-10	0111-0001-20	1
-10	0320-0001	1
-10	0112-0003	1

RG 9/25/78
T McCann 9-27-78
DRS 1-6-89
[illegible] 1/6/83
[illegible] 1/6/83

HANDLE ASSEMBLY

0111-0016 C



DWG. NO. 0285-0020
SH 1
REV R
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
G | 2759 | REV'D PER ECO & REDRAWN | JWC | DGW | 1-10-83
R | 3705 | REVISED PER E.C.O. No | JWC | DGW | 4-28-83
14
REMOVE PIN 5 FLUSH WITH CONNECTOR BASE
7 SOLDER 20 PLS
1
3 9 PLS
SOLDER SIDE
GND 3 PLS
B1
B2
B3
B4
B5
B6
B7
B8
B9
J20
COAX CONNECTIONS
J20-1 TO B2
J20-2 TO B4
J20-3 TO B3
-10 0285-0019 1
DASH NO | NUMBER | QTY
NEXT ASSEMBLY
-08 -04 -03 -02 -01
PART NUMBER | PART NAME | DESCRIPTION/SPECIFICATION | ITEM
DO NOT SCALE DRAWING
TOLERANCE
ENG. SERV | DATE
DRAWN JW CARROLL | DATE 1-10-83
CHECKED DGW
PROJ ENG. DES
MANUFACTURING
QUALITY ASSUR
GOULD Instruments Division Santa Clara Operations
TITLE ASSEMBLY 4500 MOTHER BD
SCALE 1/1 | SIZE D | PART NUMBER 0285-0020 | REV R
MODEL 4500 | SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
							0285-0022	FAB			4500 MOTHER BD	
2						1	3000-1200	RESISTOR	R1		120Ω 1/4W 5%	
3						9	6000-0394	BNC	B1-B9			
4						7	6000-0393	CONNECTOR	J1-7		80 PIN DIP	
5						3	6000-0270	CONNECTOR	J9-11		50 PIN DIP	
6												
7						1	0285-0346	CABLE ASSY			20 CONN	
8						2	6000-0390	HEADER	J16,17		26 PIN DIP	
9						1	6000-0385-06	HEADER	J14		6 PIN	
10						1	6000-0388	HEADER	J12		26 PIN, R-ANGLE	
11						1	6000-0389	HEADER	J19		34 PIN	
12						1	6000-0023	CONNECTOR	J18		4 PIN	
13						4	6100-0154	SOCKET	J18		PL SOCKET	
14						1	0285-0333	CABLE ASSY				LM
15						3	4000-0025	CAPACITOR	C1,C2,C3		.1UF, 50V, 20%	
16												
17												
18												

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
P	REVISED PER ECO No 2746	1-8-83	JWL	DGW	2-14-83
Q	REVISED PER ECO No 2759	1-8-83	JWL	DGW	2-14-83
R	REVISED PER ECO No 3705	1-8-83	JWL	DGW	
L	REVISED PER ECO 2672	[illegible]	[illegible]	DGW	
M	REVISED PER ECO # 2680	1-2-83	JWL	DGW	
N	REVISED PER ECO # 2714	2-23-83	JWL	DGW	
N	PROD REL PER ERN No 262	2-28-83	DGW	DGW	

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	S. RODELL	4-7-80
CHECKED	DGW	1-14-83
ENGINEER	DRS	1-6-83
MANUFACTURING	[illegible]	1/6/83
QUALITY ASSURANCE	[illegible]	1/6/83

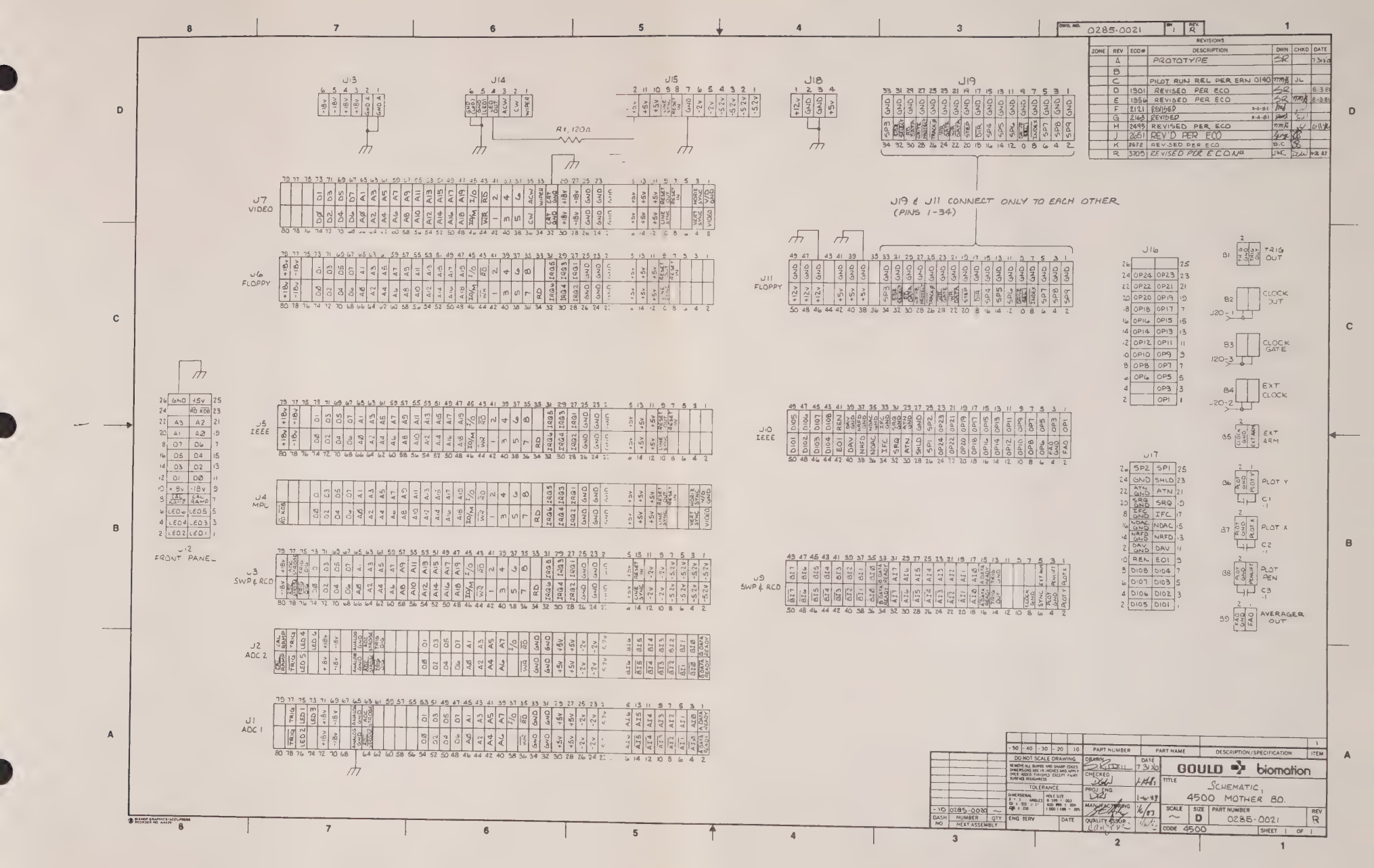
LIST OF MATERIAL
ASSEMBLY,
4500 MOTHER BD.

biomation

B | 0285-0020 | REV R

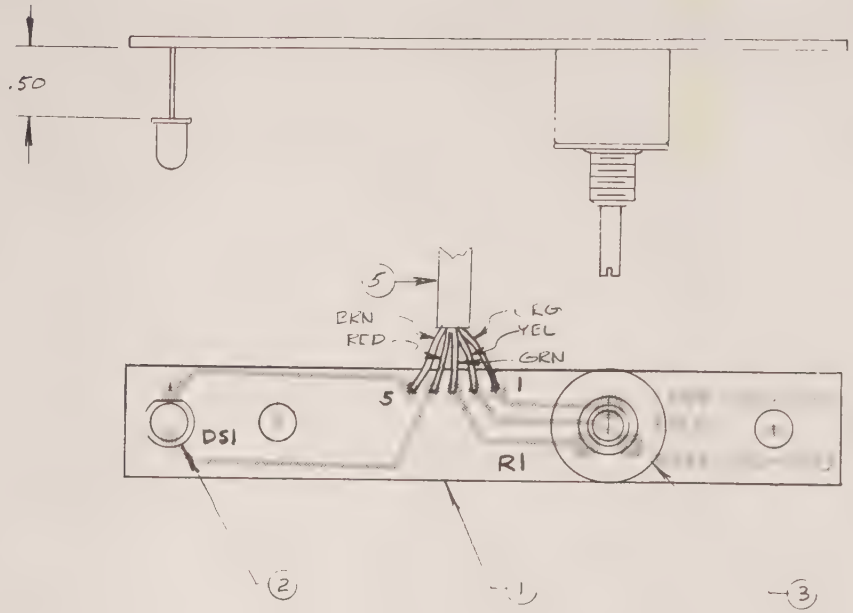
MODEL 4500

CODE | SHEET | OF


DWG. NO. 0285-0021
SH 1
REV R
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
A PROTOTYPE
B
C PILOT RUN REL PER ERN 0140 JL
D 1901 REVISED PER ECO 8-3-81
E 1956 REVISED PER ECO 8-3-81
F 2121 REVISED 9-4-81
G 2149 REVISED 9-4-81
H 2495 REVISED PER ECO
J 2651 REV'D PER ECO
K 2672 REVISED PER ECO
R 3705 REVISED PER ECO
J13
J14
J15
J18
J19
R1, 120Ω
J19 & J11 CONNECT ONLY TO EACH OTHER (PINS 1-34)
J7 VIDEO
J6 FLOPPY
J11 FLOPPY
J16
J17
J5 IEEE
J4 MPC
J10 IEEE
J12 FRONT PANEL
J3 SWP & RCD
J9 SWP & RCD
J2 ADC 2
J1 ADC 1
TRIG OUT
CLOCK OUT
CLOCK GATE
EXT CLOCK
EXT ARM
PLOT Y
PLOT X
PLOT PEN
AVERAGER OUT
C1
C2
C3
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR.
ENG SERV
DATE
GOULD biomation
TITLE
SCHEMATIC, 4500 MOTHER BD.
SCALE
SIZE D
PART NUMBER 0285-0021
REV R
CODE 4500
SHEET 1 OF 1
-10 0285-0030
DASH NO
NUMBER
NEXT ASSEMBLY
QTY

DWG. NO. 0285-0130 | SH 1 | REV. B

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
A		PILOT REL PER ERN 135 PROD. REL PER ERN 262	DRS JG	TM	4.1.83
B	2736	REVISED PER ECO N°	WC		2-14-84



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: x ± 1 ANGLES; xx .020 ± 1°; xxx ± .010
HOLE SIZE: 0 599 ± .003; 600 999 ± .004; 1 000 1 499 .005

DRAWN	DATE
SANDELL	6-2-80
CHECKED DGW	1-10-83
PROJ. ENG. DKJ	1-6-83
MANUFACTURING	1/6/83
QUALITY ASSUR	1/6/83

GOULD biomation

TITLE CRT INTENSITY PWB ASSY

SCALE	SIZE	PART NUMBER	REV
2 X	B	0285-0130	B

CODE 4500 SHEET 1 OF 1

DASH NO.	NUMBER	QTY
-10	0285-0105	1
	NEXT ASSEMBLY	

ENG. SERV. DATE

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-4427

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0285-0132	CRT INTENSITY PWB				
2						1	6400 -0039	LED			RED	
3						1	3500 - 1035	POT				
4												
5						1	0285-0124	CABLE ASSY CRT				LM

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL PER ERN 135	6-2-80	DRS	RD	
A	PROD. REL PER ERN 262	5-17-82	[illegible]		
B	REVISED PER ECO # 2736	2-14-83	[illegible]	[illegible]	

DASH NO	NUMBER	QTY
-10	0285-0105	1

NEXT ASSEMBLY

		DATE
DRAWN	SANDELL	6-2-80
CHECKED	DGW	1-10-83
ENGINEER	DRS	1-6-83
MANUFACTURING	[illegible]	1/6/83
QUALITY ASSURANCE	[illegible]	1/6/83

LIST OF MATERIAL
CRT INTENSITY
PWB ASSY

biomation

B 0285-0130 REV B

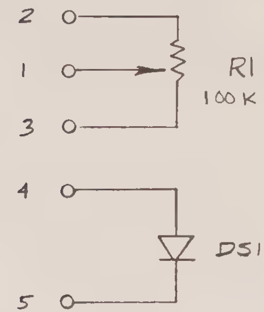
MODEL 4500

CODE

SHEET 1 OF 1

DWG. NO. 0285-0131 | SH 1 | REV. A

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
A		PILOT REL PER ERN 135	DS	RD	5/11/81



								1
–50	–40	–30	–20	–10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DASH NO.	NUMBER	QTY
–10	0285-0130	—
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°

HOLE SIZE: 0 .599 ± .003; .600 .999 ± .004; 1.000 1.499 ± .005

ENG. SERV. | DATE

		DATE
DRAWN	SANDELL	5-8-81
CHECKED	DGW	1-10-83
PROJ. ENG.	DRS	1-6-83
MANUFACTURING	[signature]	1/6/83
QUALITY ASSUR.	[signature]	1/-/83

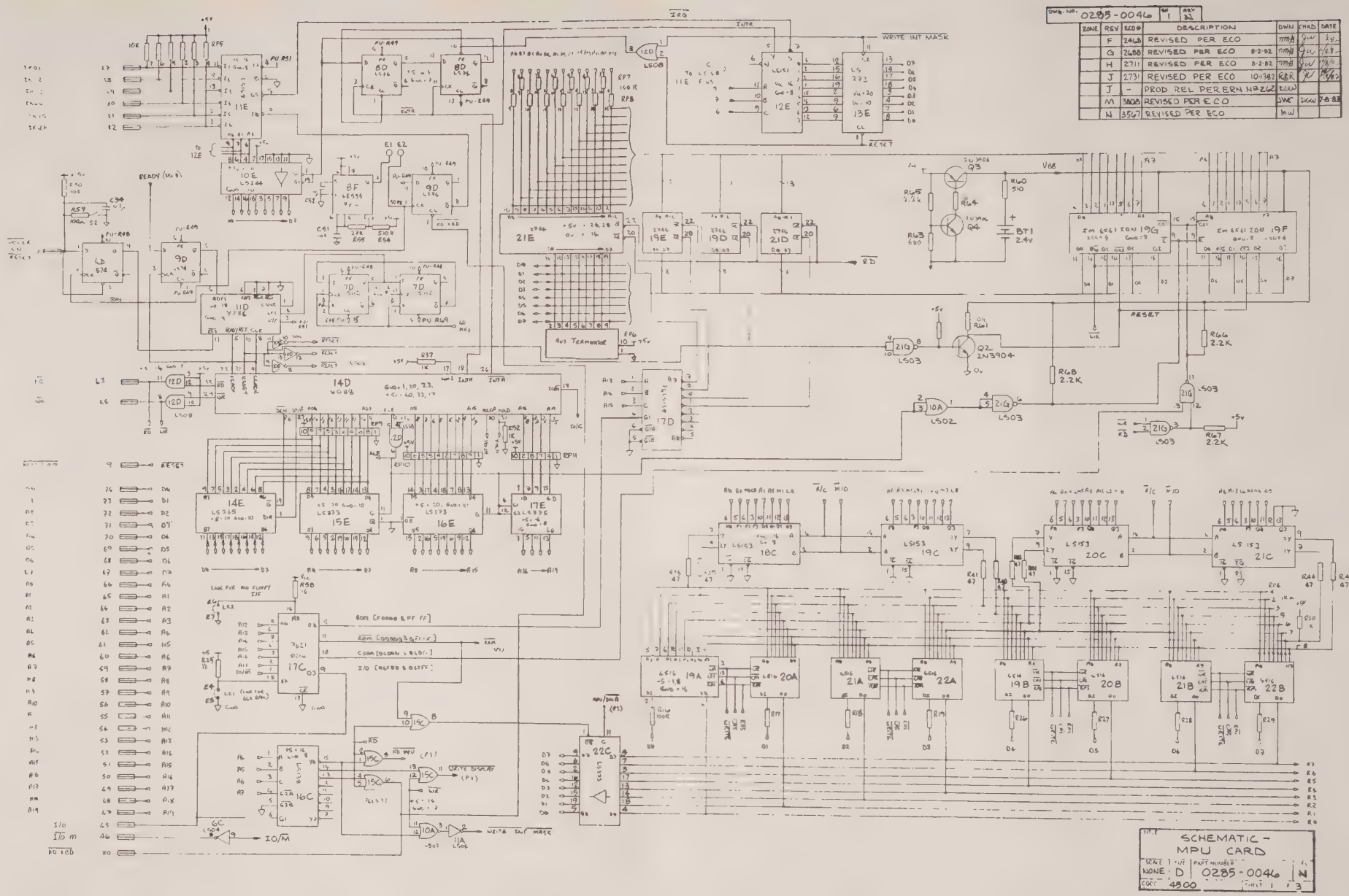
GOULD biomation

TITLE CRT INTENSITY SCHEM.

SCALE	SIZE	PART NUMBER	REV
	B	0285-0131	A

CODE T100-A | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4427



DWG. NO. 0285-0046
SH 1
REV N
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
F 2468 REVISED PER ECO
G 2688 REVISED PER ECO 8-2-82
H 2711 REVISED PER ECO 8-2-82
J 2731 REVISED PER ECO 10-13-82
J - PROD REL PER ERN NO 262
M 3808 REVISED PER ECO
N 3567 REVISED PER ECO
WRITE INT MASK
RESET
READY
BUS TERMINATOR
ROM [FOOOO & FF FF]
RAM [GGGGG & GFFFF]
CRAM [GGGGG & GGGFF]
I/O [GGGGG & GGGFF]
WRITE DISPLAY
WRITE INT MASK
SCHEMATIC - MPU CARD
SCALE NONE
SIZE D
PART NUMBER 0285-0046
N
CODE 4500
SHEET 1 OF 3

DWG NO 0285-00046 | SH 2 | REV N

REVISIONS					
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	B		PILOT REL PER ERN 139		JL	
	C	2004	REVISED PER ECO			
	D	2114	REVISED PER ECO			
	E	2322	REVISED PER ECO			

LRM INITIATION LOGIC

MPU RAM REQ

TRACE REQ GEN

MPU RAM OPN

TRACE LATCH

TRACE RAMD GEN.

MPU/DMA

TRACE REQ

MID (RAM MPU ADDRESS SEL)

TRACE QUART (P3)

LOAD LAST TRACE STORE (P1)

TRACE REQ

TRACE / CHARACTER ADDRESS MULTIPLEX

COU ENAB (P3)

MIDDLE OF CHR (P3)

LD TRA COU

BOTTOM OF SCREEN

MPU/DMA

RMS ENAB

16k RAM CONTROL LOGIC

RAS (P1)

CAS (P1)

WRITE (P)

MPU RAM OPN

R/C (P1)

NOTE R/C MISSING IN CR6 W

H BLANK (3F-1)

V SYNC

H BLANK (P5)

LOAD LINE COUNT

DISPLAY COUNTER

Note: 1. ALL SCHOTTKY OUTPUTS TO HAVE 47 OHM RESISTOR IN SERIES, AT SENDING END

2. 19D&E, 21D&E NOT LOADED

DASH NO	NUMBER	QTY	NEXT ASSEMBLY

ENG SERV	DATE

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING & FINISH EXCEPT WHERE OTHERWISE SPECIFIED
SURFACE ROUGHNESS

TOLERANCE

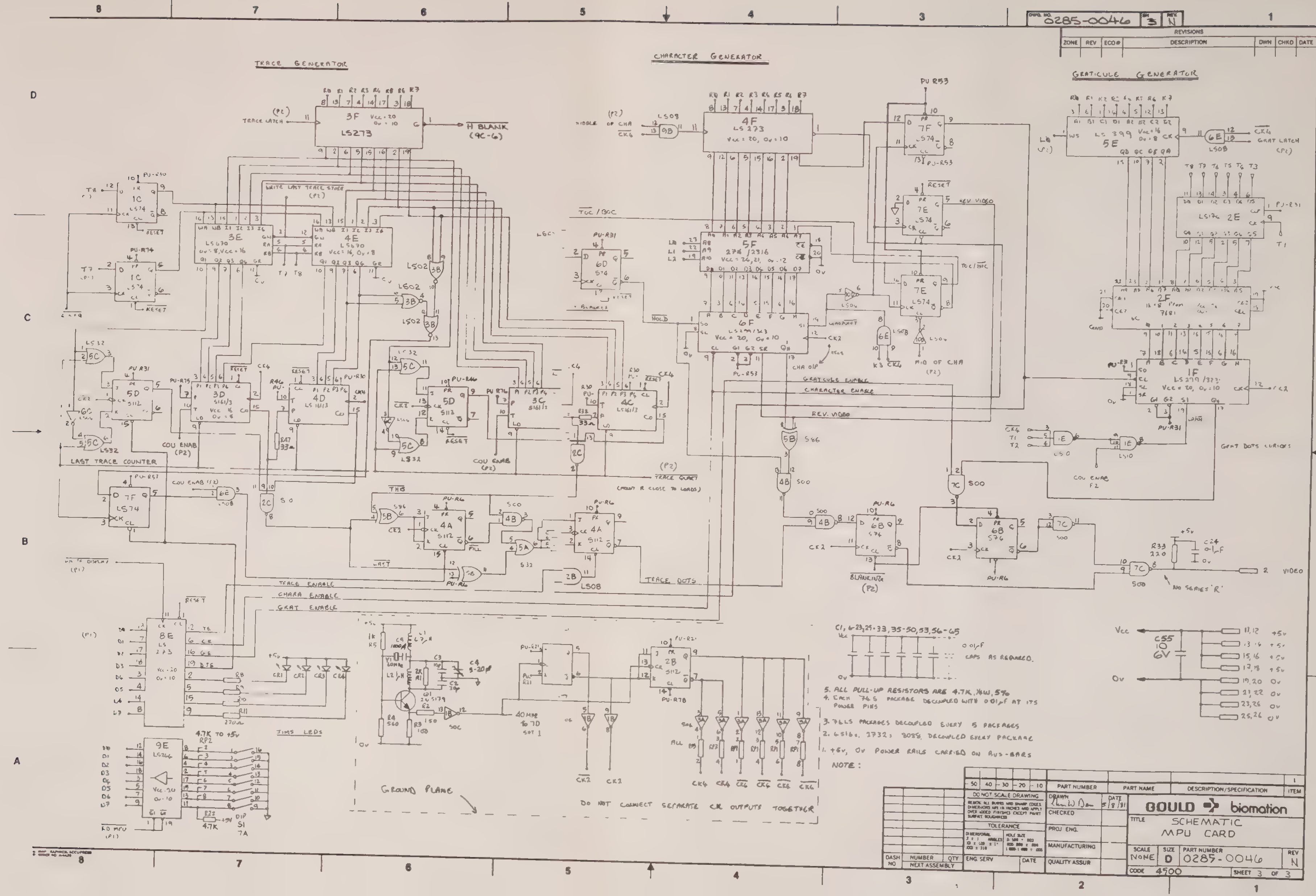
DRAWN C.M. & W.J.W. DATE 5/8/74
CHECKED 1/14/75
PROJ ENG 1-16-75
MANUFACTURING 1/16/75
QUALITY ASSUR 1/16/75

GOULD biomation

TITLE SCHEMATIC MPU CARD

SCALE | SIZE D | PART NUMBER 0285-00460 | REV N

CODE 4500 | SHEET 2 OF 3

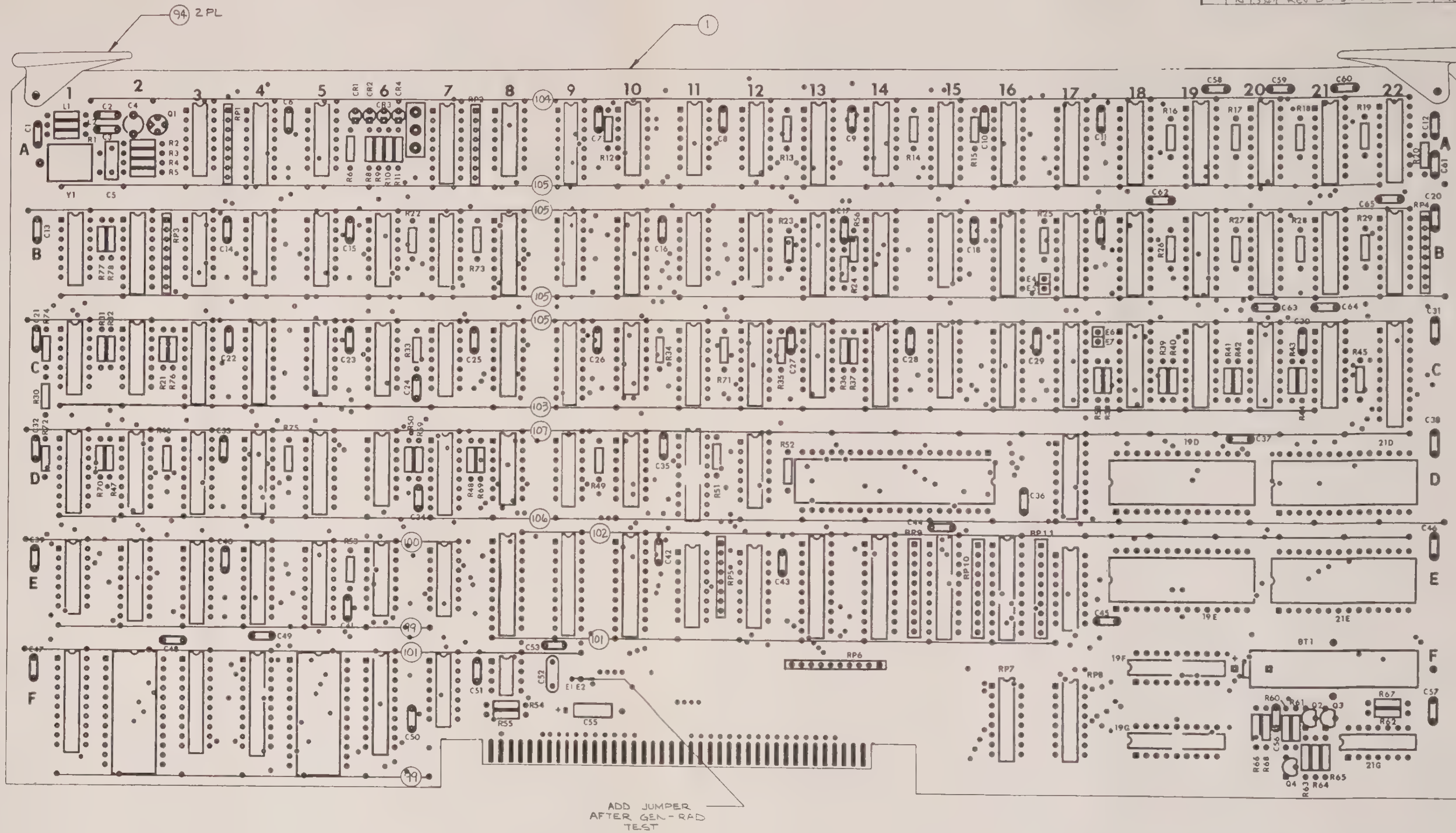


0285-0046
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
TRACE GENERATOR
CHARACTER GENERATOR
GRATICULE GENERATOR
3F LS273
H BLANK (9C-6)
4F LS273
5E LS 399
3E LS670
4E LS670
5F 2716/2316
6F LS299/323
2E LS174
2F 7681
1F LS299/323
WRITE LAST TRACE STORE (P2)
LAST TRACE COUNTER
COU ENAB (P2)
TRACE QUIET (P2)
TRACE ENABLE
CHARA ENABLE
GRAT ENABLE
GRATICULE ENABLE
CHARACTER ENABLE
REV. VIDEO
TRACE DOTS
BLANKING (P2)
GRAT DOTS CURSORS
VIDEO
NO SERIES 'R'
8E LS 273
9E LS244
JIMS LEDS
4.7K TO +5V
GROUND PLANE
40 MHz
DO NOT CONNECT SEPARATE CK OUTPUTS TOGETHER
C1, 6-23, 25-33, 35-50, 53, 56-65
0.01µF CAPS AS REQUIRED.
C55 10 6V
NOTE:
1. +5V, 0V POWER RAILS CARRIED ON BUS-BARS
2. 6516s, 2732s, 8085 DECOUPLED EVERY PACKAGE
3. 74LS PACKAGES DECOUPLED EVERY 5 PACKAGES
4. EACH 74S PACKAGE DECOUPLED WITH 0.01µF AT ITS POWER PINS
5. ALL PULL-UP RESISTORS ARE 4.7K, ¼W, 5%
DO NOT SCALE DRAWING
TOLERANCE
GOULD biomation
TITLE SCHEMATIC MPU CARD
DATE 5/8/81
SCALE NONE
SIZE D
PART NUMBER 0285-0046
REV N
CODE 4500
SHEET 3 OF 3

DWG. NO. 0285-0045	SH 1	REV N

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	—	—	[illegible]	[illegible]		
	N	3541	REV'D PER ECO	[illegible]		



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

CRAWN 7 M Grelle	DATE 4/7/81
CHECKED DGW	1-14-81
PROJ ENG. [illegible]	[illegible]
MANUFACTURING [illegible]	1/1/82
QUALITY ASSUR	

DASH NO | NUMBER | QTY — NEXT ASSEMBLY

ENG SERV | DATE

GOULD biomation

TITLE ASSEMBLY — MPU BD.

SCALE	SIZE	PART NUMBER	REV
2/1	D	0285-0045	N

CODE 4500 SHEET 1 OF 1

BISHOP GRAPHICS ACCUPRESS

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -50	-40	-30	-20	-10	-05	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1					—	1	0285-0047	FABRICATION				
2					1	—	0285-0145-05	MPU PCB				
3												
4					—	1	1800-0192	I.C.	21G	74LS03		
5					—	2	1800-0031	"	4B, 7C	74S00		
6					—	1	-0105	"	12A	74LS00		
7					—	2	-0106	"	3B, 10A	74LS02		
8					—	2	-0092	"	1B, 3A	74S04		
9					—	3	-0107	"	6C, 10D, 11A	74LS04		
10					—	4	-0109	"	12D, 12B, 9B, 6E	74LS08		
11					—	1	-0060	"	2C	74S10		
12					—	1	-0110	"	1E	74LS10		
13					—	2	-0214	"	10C, 15B	74LS11		
14					—	1	-0275	"	14A	74LS21		
15					—	1	-0244	"	5A	74S32		
16					—	3	-0216	"	15C, 5C, 8A	74LS32		
17					—	1	-0113	"	13C	74LS54		
18					—	2	1800-0054	I.C.	6B, 6D	74S74		

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE				
B	PILOT REL PER ERN 0139	5-7-81	[illegible]	JL	
C	REVISED PER ECO #1840	[illegible]	[illegible]	RG	
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
F	REVISED PER ECO #2322	[illegible]	[illegible]	[illegible]	
G	REVISED PER ECO 2425	[illegible]	[illegible]	[illegible]	

	DRAWN	DATE
	CHECKED DGW	1-10-83
	ENGINEER	
	MANUFACTURING	1/6/83
	QUALITY ASSURANCE	

DASH NO | NUMBER | QTY
NEXT ASSEMBLY

LIST OF MATERIAL
ASSEMBLY
MPU BD

biomation

B | 0285-0045 | REV G

MODEL 4500 | CODE | SHEET 1 OF 7

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19						8	1800-0115	I.C.	1C, 7B, 7E, 7F, 8C, 8D, 9D, 11B	74LS74		
20						1	-0206	"	5B	74S86		
21						4	-0039	"	7D, 5D, 4A, 2B	74S112		
22						9	-0068	"	8B, 9C, 10B, 12C, 13A, 13B, 14B, 15A, 16B	74LS112		
23						2	-0193	"	17D, 16C	74LS138		
24						1	-0332	"	11E	74LS148		
25						1	-0181	"	12E	74LS151		
26						4	-0217	"	18C, 19C, 20C, 21C	74LS153		
27						2	-0213	"	17A, 18A	74LS157		
28						2	-0208	"	3C, 3D	74S161		
29						9	-0125	"	4C, 4D, 2D, 1D, 9A, 11C, 16A, 17B, 18B	74LS161		
30						1	-0190	"	2E	74LS174		
31						1	-0330	"	14C	74LS195		
32						2	-0240	"	9E, 10E	74LS244		
33						1	-0268	"	14E	74LS245		
34						4	-0231	"	13E, 4F, 8E, 3F	74LS273		
35						2	-0333	"	1F, 6F	74LS299		
36						3	1800-0298	I.C.	22C, 15E, 16E	74LS373		

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
H	REVISED PER ECO # 2468	7/31/82	[illegible]	AW	
J	REVISED PER ECO # 2688	8/2/82	[illegible]	[illegible]	
K	REVISED PER ECO # 2711	8/2/82	[illegible]	[illegible]	
L	REVISED PER ECO # 2731	10/13/82	[illegible]	[illegible]	
L	PROD REL PER ERN N# 262	12-20-82	DGW	[illegible]	
M	REVISED PER ECO N# 3006	7-8-83	DGW	[illegible]	7-13-83
N	REVISED PER ECO # 3507	11-7-83	MW	[illegible]	

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

DASH NO. | NUMBER | QTY
NEXT ASSEMBLY

LIST OF MATERIAL
ASSEMBLY
MPU BD

biomation

B | 0285-0045 | REV N

MODEL 4500 | CODE | SHEET 2 OF 7

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
37												
38						1	1800-0337	I.C.	17E	74LS375		
39						1	1800-0338	I.C.	5E	74LS399		
40						2	1800-0220	I.C.	3E,4E	74LS670		
41						1	0285-0370-01	CHR PROM	5F			
42												
43						8	1800-0320	I.C.	19A,19B,20A,20B 21A,21B,22A,22B	4516		
44						1	0285-0371-01	MAP PROM	17C			
45						1	0285-0372-01	GRA. PROM	2F			
46						1	1800-0339	I.C.	14D	8088		
47						1	1800-0327	I.C.	11D	8284		
48						1	1700-0078	I.C.	8F	NE555		
49						2	1820-0074	I.C.	19F,19G	IM6561		
50												
51												
52						1	1300-0007	TRANSISTOR	Q1	2N5179		
53						2	1300-0028	TRANSISTOR	Q2,4	2N3904		
54						1	1400-0019	TRANSISTOR	Q3	2N3906		

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
MPU BD

biomation

B | 0285-0045 | REV N

MODEL 4500 | CODE | SHEET 3 OF 7

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55						2	3700-0076	RES PACK	RP1,3		47Ω, 8 PIN	4 RES
56						2	3700-0074	"	RP7,8		100Ω, 16 PIN	8 RES
57						1	3700-0016	"	RP4		1K, 8 PIN	7 RES
58						1	3700-0015	"	RP5		10K 8 PIN	7 RES
59						1	3700-0041	"	RP2		4.7K, 8 PIN	7 RES
60						4	3700-0049	RES PACK	RP6 9,10,11		3K/6.2K, 10 PIN	8 RES
61												
62						5	3000-3306	RESISTOR	R23,24,32,47,56		33Ω, 1/4W, 5%	
63						8	-4706	"	R38,39,40,41, 42,43,44,45		47Ω,	
64						10	-1000	"	R3,16,17,18,19,26, 27,28,29,39		100Ω,	
65						26	-4701	"	R6,12,13,14,15,21,30,31,35,36 46,48,49,51,53 22,69-78		4.7K	
66						1	-5100	"	R60		510Ω	
67						1	-1500	"	R2		150Ω	
68						5	-2200	"	R8,9,10,11,33		220Ω	
69						1	-5600	"	R4		560Ω	
70						7	-1001	"	R5,20,25,37,52, 58,64		1K	
71						1	-2001	"	R1		2K	
72						3	3000-1002	RESISTOR	R34,50,61		10K, 1/4W, 5%	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
MPU BD

biomation

B | 0285-0045 | REV N

MODEL 4900 | CODE | SHEET 4 OF 7

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
73						1	3000-2702	RESISTOR	R55		27K, 1/4W, 5%	
74												
75						1	-5103		R54		510K,	
76						5	-2201		R62, 65-68		2.2K,	
77												
78						1	3000-6800	RESISTOR	R63		680Ω, 1/4W, 5%	
79						56	4000-0005	CAPACITOR	C1, 6-23, 25-33, 35-50, 52, 53, 56-65		.01μf	
80						1	4000-0029		C51		.05μf, 100V	
81						2	4000-0025		C24, 34		.1μf, 50V	
82						1	4400-0039		C55		10μf, 6V	
83						1	4100-0005		C3		10pf 500V	
84						1	4100-0029		C2		30pf 500V	
85						1	4100-0015	CAPACITOR	C5		1000pf, 500V	
86						1	4600-0012	VAR CAP	C4		5-20 pf,	
87												
88						1	5100-0019	CRYSTAL	Y1		40 MHZ	
89												
90						4	6400-0039	LED	CR1 THRU 4		RED	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
MPU BD

biomation

B | 0285-0045 | REV N

MODEL 4900 | CODE | SHEET 5 OF 7

COMMENTS	TOTAL COST	UNIT COST
NOTE: FOR ITEM 108		
(LITH ION BATTERY);		
SPECIAL HANDLING IS		
REQD THROUGHOUT		
INTERNAL PROCESSING		

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY 60	50	40	30	20	10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
91						1	6600-0078	SWITCH	S2		PUSH DPDT	
92						1	6600-0037	SWITCH	S1		8 POS. DIP	
93												
94						2	7000-0120	EJECTOR				
95												
96						1	2100-0005	INDUCTOR	L2		1 uh	
97						1	2100-0002	INDUCTOR	L1		4.7 uh	
98												
99						2	9000-0094-01	BUSS BAR			7 PIN .65 SP.	
100						1	-02				8 PIN	
101						2	-03				10 PIN	
102						1	-04				15 PIN	
103						1	-05				21 PIN	
104						1	-06				22 PIN	
105						4	-07				23 PIN .65 SP.	
106						1	-08				23 PIN PIN 11 REMOVED	
107						1	9000-0094-09	BUSS BAR			23 PIN PIN 12 REMOVED	
108						1	7000-0451	BATTERY	BT1		2.4V LITHIUM	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
MPU BD

biomation

B | 0285-0045 | REV N

MODEL 4900 | CODE | SHEET 6 OF 7

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
109												
110												
111												
112												
113												
114						1	7200-0031	MOUSE TAIL				
115						9	6100-0120	SOCKET	19-22(A&B),17C		16 PIN	
116						3	6100-0156	SOCKET	11D,19F,19G		18 PIN	
117						2	6100-0122	SOCKET	F2,F5		24 PIN	
118						1	6100-0123	SOCKET	14D		40 PIN	
119												
120												
121												
122												
123												
124												
125												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

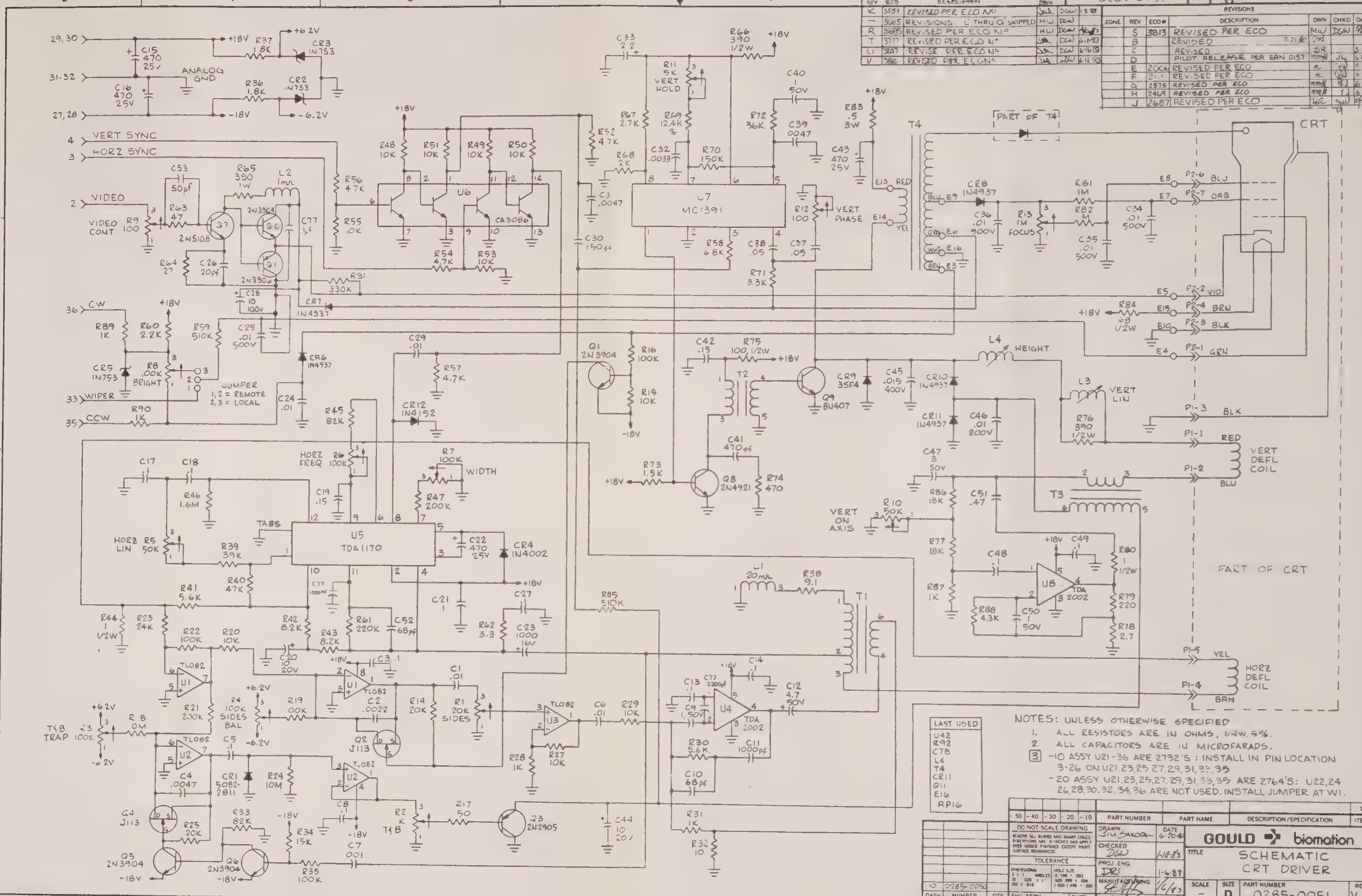
	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
MPU BOARD

biomation

B | 0285-0045 | REV N

MODEL 4500 | CODE | SHEET 7 OF 7



REV	ECO	DESCRIPTION	DWN		
K	3559	REVISED PER ECO No		DGW	1 5 83
—	3605	REVISIONS 'L' THRU 'Q' SKIPPED	MW	DGW	
R	3685	REVISED PER ECO No	MW	DGW	
T	3777	REVISED PER ECO No		DGW	6-16-83
U	3847	REVISE PER ECO No		DGW	6-16-83
V	3860	REVISED PER ECO No		DGW	6-16-83

DWG NO. 0285-0051 SH 1 REV V

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	S	3813	REVISED PER ECO	MW	DGW	
	B		REVISED 7-21-80			
	C		REVISED	SR		3-11-81
	D		PILOT RELEASE PER ERN 0157		JL	
	E	2006	REVISED PER ECO			
	F	2111	REVISED PER ECO		GW	
	G	2375	REVISED PER ECO			
	H	2469	REVISED PER ECO			
	J	2687	REVISED PER ECO		GW	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. -10 ASSY U21-36 ARE 2732'S : INSTALL IN PIN LOCATION 3-26 ON U21,23,25 27,29,31,33,35
   -20 ASSY U21,23,25,27,29,31,33,35 ARE 2764'S: U22,24 26,28,30,32,34,36 ARE NOT USED. INSTALL JUMPER AT W1.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

-10	0285-0050	
DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1, .XX ± .020, .XXX ± .010; ANGLES ± 1°

HOLE SIZE: 0-.599 ± .003; .600-.999 ± .004; 1.000-1.499 ± .005

ENG SERV — DATE

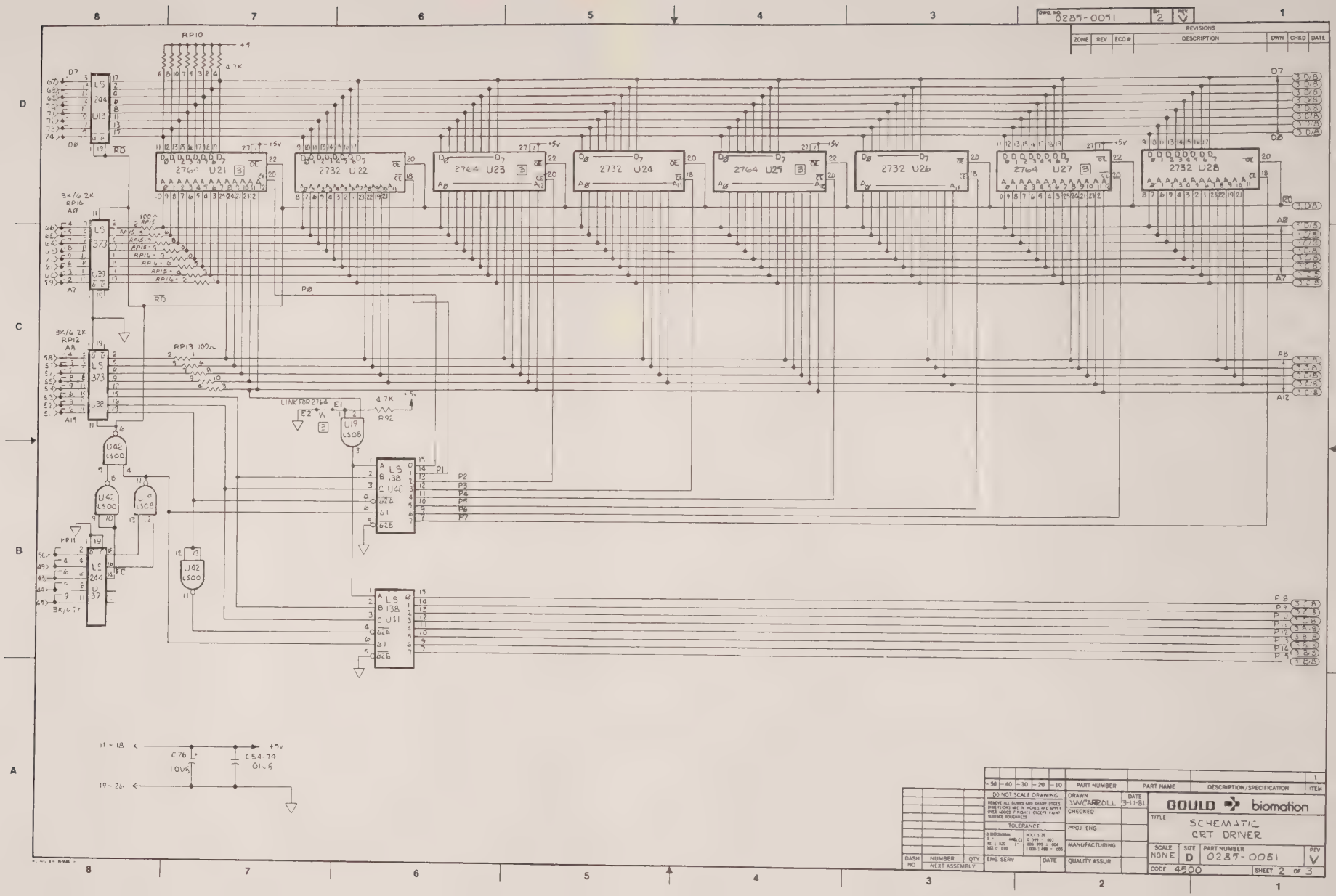
		DATE
DRAWN	JIM SAKODA	6-20-80
CHECKED	DGW	1-10-83
PROJ ENG	DRS	1-6-83
MANUFACTURING		1/6/83
QUALITY ASSUR		1/5/83

GOULD biomation

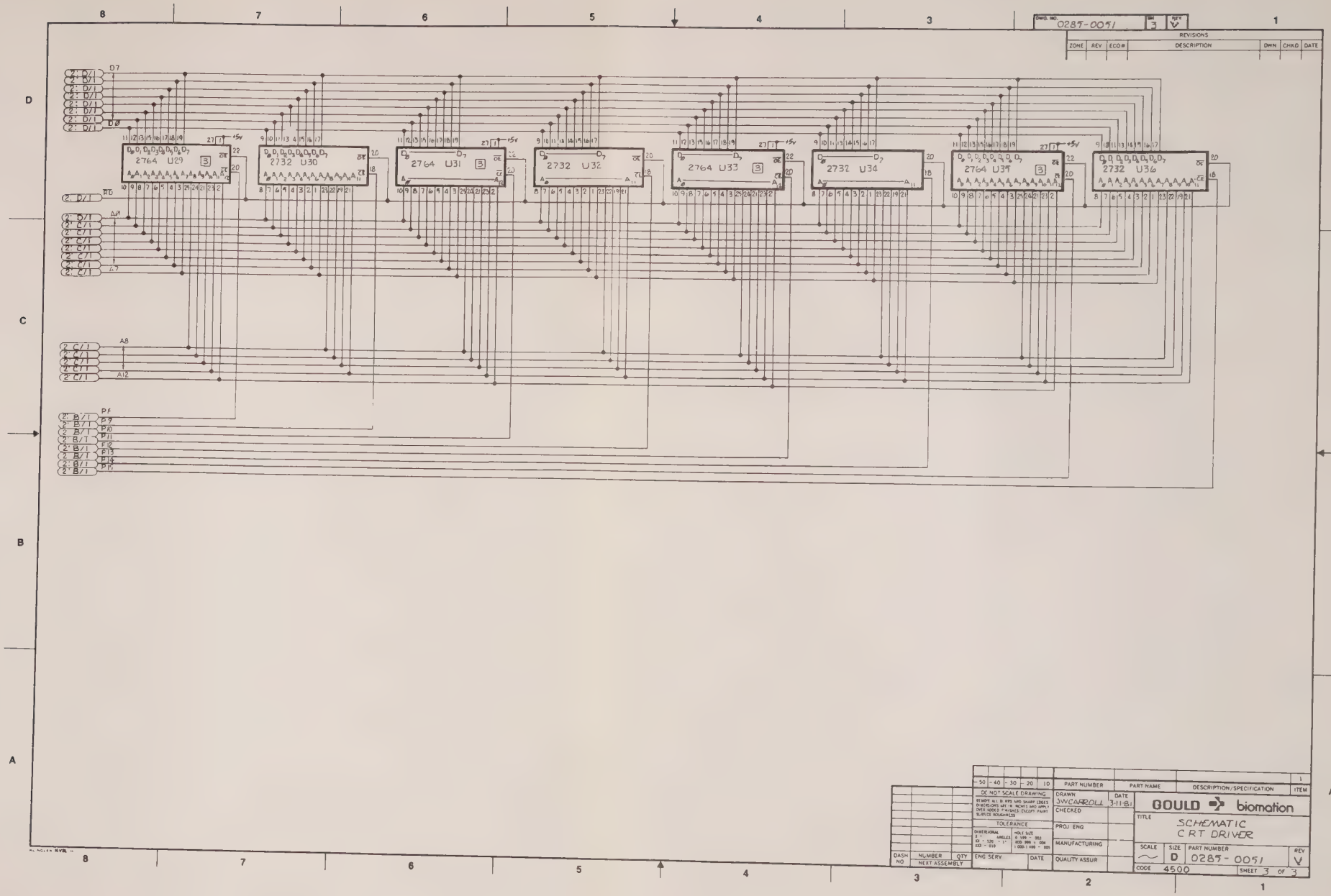
TITLE SCHEMATIC CRT DRIVER

SCALE – SIZE D PART NUMBER 0285-0051 REV V

CODE 4500 SHEET 1 OF 3

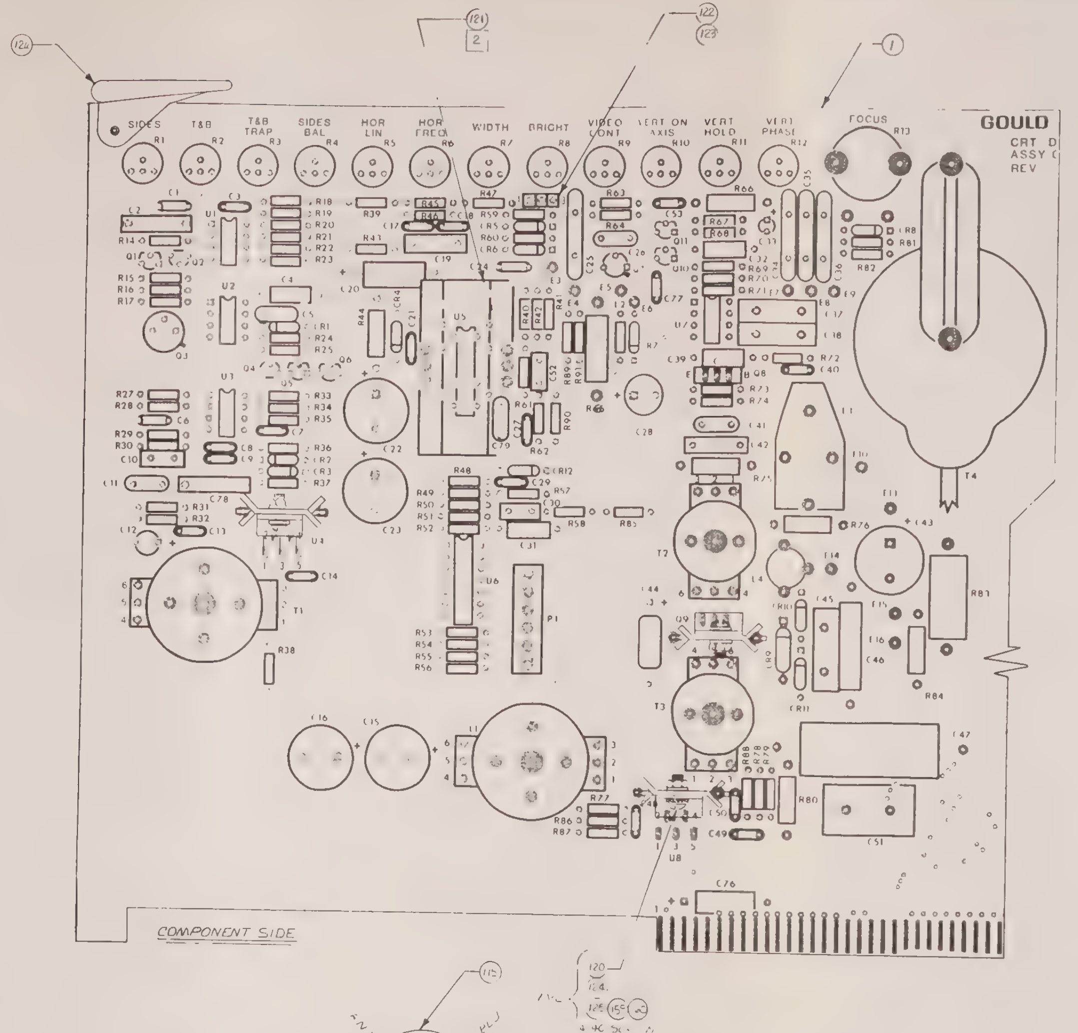


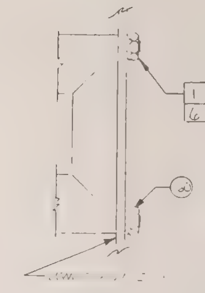
DWG. NO. 0285-0051
SH 2
REV V
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
RP10
4.7K
D7
D0
LS 244 U13
RD
2764 U21
2732 U22
2764 U23
2732 U24
2764 U25
2732 U26
2764 U27
2732 U28
3K/6.2K RP14 A0
LS 373 U39
A7
3K/6.2K RP12 A8
LS 373 U38
A15
RP13 100Ω
LINK FOR 2764
E1
E2
U19 LS08
R92
4.7K
U42 LS00
LS 138 U40
LS 138 U41
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
RP11
LS 244 U37
FE
11 - 18
19 - 26
C76 10U5
C54-74 01U5
+5V
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL
HOLE SIZE
ENG. SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN JWCARROLL
DATE 3-11-81
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC CRT DRIVER
SCALE NONE
SIZE D
PART NUMBER 0285-0051
REV V
CODE 4500
SHEET 2 OF 3



DWG. NO. 0285-0051
SH 3
REV V
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
2764 U29
2732 U30
2764 U31
2732 U32
2764 U33
2732 U34
2764 U35
2732 U36
D7
D0
A0
A7
A8
A12
P7
P10
P11
P12
P13
P14
P15
2: D/1
2: C/1
2: B/1
+5V
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
JWCARROLL
DATE
3-11-81
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
SCHEMATIC
CRT DRIVER
SCALE
SIZE
D
PART NUMBER
0285-0051
REV
V
CODE
4500
SHEET 3 OF 3

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	–	–	SEE HISTORY	MW		
	W	4065	REVISED PER ECO №	MW	DGW	[illegible]
	X	[illegible]	[illegible]			
	Y	4176	REVISED PER ECO №	DGW	[illegible]	[illegible]
	Z	4352	REVISED PER ECO 4352	MW	[illegible]	[illegible]
	AA	4362	REVISED PER ECO 4362	MW	[illegible]	[illegible]





FROM	TO		LGTH
P2-1	E4		
P2-2	E5		
P2-3	[illegible]		
P2-4	[illegible]		
P2-5	[illegible]		
P2-6	[illegible]		
P2-7	[illegible]		
T4-BRN	[illegible]		
T4-WHT	[illegible]		
T4-ORG	[illegible]		
T4-BLU	[illegible]		
T4-YEL	[illegible]		
T4-RED	[illegible]		

NOTES: UNLESS OTHERWISE SPECIFIED

1. TIGHTEN [illegible] IN [illegible]
2. INSTALL HEATSINK WITH THE TABS AS SHOWN.
3. -20 ASSY: INSTALL U21,23,25,27, 29,31,33,35 ONLY AS SHOWN. INSTALL C58 60,62,64,66,68,70,77 ONLY AS SHOWN. INSTALL ITEM 134.
4. -10 ASSY: INSTALL U21,23,25,27 [illegible] IN PIN LOCATION 3 AND 26. INSTALL ALL OTHER COMPONENTS AS SHOWN.
5. [illegible]
6. [illegible] FOR SCREW OR THREADS TO BE FLUSH WITH HEXNUT.

20	[illegible]	1
10	2285-0002	1
DASH NO	NUMBER / NEXT ASSEMBLY	QTY

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE: DIMENSIONAL .X ± .1, .XX ± .020, .XXX ± .010, ANGLES ± 1°; HOLE SIZE 0 .599 - .003, .600 .999 - .004, 1.000-1.490 - .005

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

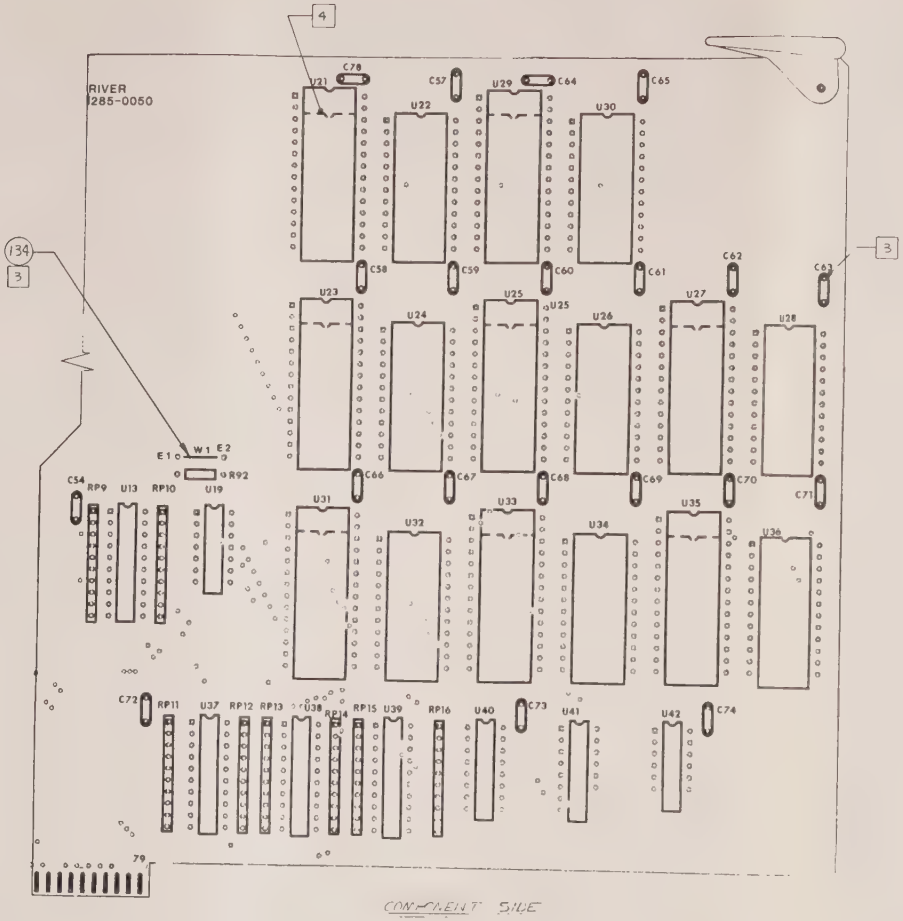
DRAWN J.W.CARROLL DATE 6-12-81
CHECKED DGW 1-14-82
PROJ. ENG. DRS
MANUFACTURING SEH 1/6/83
QUALITY ASSUR
ENG SERV DATE

GOULD biomation

TITLE: ASSEMBLY CRT DRIVER

SCALE 2/1 | SIZE D | PART NUMBER 0295-[illegible] | REV AA

CODE 4500 | SHEET 1 OF 2



DWG. NO. 0285-0050 SH 2 REV AA

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHEET 1			

-50	-40	-30	20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = ± ANGLES; XX = ± .020 ± 1°; XXX = ± .010

HOLE SIZE: 0.599 ± .003; 0.500 .999 ± .004; 1.000 1.499 ± .005

ENG SERV. DATE

DASH NO	NUMBER	QTY
-20	0285-0002	1
-10	0285-0002	1

NEXT ASSEMBLY

DRAWN J.W.CARROLL DATE 6-2-81

CHECKED

PROJ ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE ASSEMBLY CRT DRIVER

SCALE 2/1 SIZE D PART NUMBER 0285-0050 REV AA

CODE 4500 SHEET 2 OF 2

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1					1	1	0285-0052	P.W.B.				
2												
3												
4					3	3	1700-0083	I.C.	U1,2,3	TL0-82		
5					1	1	1700-0094	"	U5	TDA-1170		
6					1	1	1700-0081		U7	MC1391P		
7					2	2	1700-0093	"	U4,8	TDA2002A		
8					1	1	1700-0080	I.C.	U6	CA3086		
9												
10												
11					4	4	1300-0028	TRANSISTOR	Q1,5,6,10	2N3904		
12					1	1	1400-0003	"	Q3	2N2905		
13					1	1	1300-0048		Q8	2N4921		
14					1	1	1300-0049		Q9	BU407		
15					1	1	1300-0040		Q7	2N5108		
16					2	2	1500-0008	"	Q2,4	J113		
17					1	1	1400-0019	TRANSISTOR	Q11	2N3906		
18					16	-	4000-0005	CAPACITOR	24,29,54-58,60,62,64-66,68,70,72-74		.01 μf, 100V	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE	2-9-81	MF		
B	REVISED	3-25-81	MF		
C	REVISED	3.9.81	SR		
D	PILOT RELEASE PER ERN 0157	6-19-81	MMG	JL	
E	REVISED PER ECO #1905	9-15-81	MMG	RG	
F	REVISED PER ECO #2008	10-8-81	MMG	JW	
G	REVISED PER ECO #2111	10-6-82	MMG	JW	

DASH NO.	NUMBER	QTY
-20	0285-0002	1
-10	0285-0003	1
NEXT ASSEMBLY		

	DRAWN	DATE
	Jim Sharon	5-29-82
	CHECKED DW	1-6-83
	ENGINEER DRS	1-6-83
	MANUFACTURING	1/6/83
	QUALITY ASSURANCE	1/6/83

LIST OF MATERIAL

CRT DRIVER

biomation

B	0285-0050	REV X

MODEL 4500 | CODE | SHEET 1 OF 2

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19					5	5	1200-0031	DIODE	CR6,7,8,10,11	IN4937		
20					1	1	1200-0001	DIODE	CR4	IN4002		
21					3	3	1100-0004	DIODE	CR5,2,3	IN753A		
22					1	1	1200-0033	DIODE	CR9	35F4		
23												
24												
25					1	1	1000-0002	DIODE	CR12	IN4152		
26					1	1	2100-0005	INDUCTOR	L2		1 mh	
27					1	1	0113-0011	" VAR.	L3		VERT LIN.	
28					1	1	0285-0227	" VAR.	L4		HEIGHT	
29					1	1	0285-0224	INDUCTOR	L1		20mh	
30					1	1	3000-3303	RESISTOR	R91		330K, 1/4W, 5%	
31					1	1	3000-2706	RESISTOR	R64		27Ω, 1/4W, 5%	
32					1	1	9000-0073	TRANSFORMER	T4		FLYBACK	
33					1	1	0113-0014	"	T2		POT CORE	
34					1	1	0285-0225	"	T3		POT CORE	
35					1	1	0285-0226	TRANSFORMER	T1		POT CORE	
36					1		3000-4301	RESISTOR	R88		4.3K, 1/4W 5%	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
H	REVISED PER ECO # 2083	10-20-81	MMG	RG	
J	REVISED PER ECO 2099	11-20-81	MMG	RG	
K	REVISED PER ECO #2438	3-24-82	JW	JW	
L	REVISED PER ECO 2375	5-27-82	MMG	JW	
M	REVISED PER ECO 2469	5-27-82	MMG	JW	
N	PROD. REL PER ERN #262	6-10-82	JW	JW	
N	REVISED PER ECO 2671	10-6-82	MMG	JW	

DASH NO	NUMBER	QTY
NEXT ASSEMBLY		

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL

CRT DRIVER

biomation

B	0285-0050	REV X

MODEL 4500 | CODE | SHEET 2 OF 2

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
37					1	1	3000-2707	RESISTOR	R78		2.7Ω, 1/4W, 5%	
38					1	1	-3307		R62		3.3Ω	
39					1	1	-9107		R38		9.1Ω	
40					1	1	-1006		R32		10Ω	
41					1	1	-4706		R63		47Ω	
42					2	2	-8201		R42,43,		8.2K	
43					1	1	-1500		R17		150Ω	
44												
45					1	1	-2200		R79		220Ω	
46					1	1	-4700		R74		470Ω	
47					3	3	-1001		R28, 89, 90		1K	
48					1	1	-1501		R73		1.5K	
49					2	2	-1801		R36,37		1.8K	
50					2	2	-2001		R68,87		2K	
51					1	1	-2201		R60		2.2K	
52					1	1	-2701		R67		2.7K	
53					1	1	-3301		R71,		3.3K	
54					4	4	3000-4701	RESISTOR	R54,R56,57,92		4.7K, 1/4W 5%	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
P	REV'D PER ECO NO. 3559	3-29	DLW	DLW	2 MAY
Q	REVISED PER ECO Nº 3586	3-8-82	DLW	[illegible]	3/8/82
R	REV'D PER ECO Nº 3685	4/25/83	MW	DLW	4/4/83
S	REV'D PER ECO 3813	5/6/83	MW	DLW	5/5/83
T	REV'D PER ECO 3777	6/1/83	DLW	DLW	6-17-83
U	REV'D PER ECO 3847	6/8/83	DLW	DLW	"
V	REV'D PER ECO 3860	6/14/83	DLW	DLW	6-17-83

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL

CRT DRIVER

biomation

B | 0285-0050 | REV X

MODEL 4500 | CODE | SHEET 3 OF 9

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55					2	2	3000-5601	RESISTOR	R41,30		5.6K, 1/4W, 5%	
56					1	1	3000-6801		R58		6.8K	
57					1	1	3000-3602	RESISTOR	R72		36K 1/4W 5%	
58					11	11	3000-1002		R15,20,27,29,48,49,50,51,52,53,55			
59					1	1	3100-1242-10		R69		12.4 K 1%	
60					1	1	3000-1502		R34		15K	
61					2	2	-2002		R14,25		20K	
62					1	1	-2402		R23		24K	
63					1	1	-3902		R39		39K	
64					1	1	-4702		R40		47K	
65					2	2	-8202		R33,45		82K	
66					4	4	-1003		R16,19,22,35		100K	
67					1	1	-1503		R70		150K	
68					2	2	-2003		R21,47		200K	
69					1	1	-5103		R59		510K	
70					2	2	-1004		R81,82		1M	
71					2	2	-1802		R77,86		18K	
72					1	1	3000-1005	RESISTOR	R18		10M, 1/4W, 5%	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
W	REV'D PER ECO # 4065	11/28/84	DLW	DLW	
X	REVISED PER ECO 4122	2/6/85	DLW		

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL

CRT DRIVER

biomation

B | 0285-0050 | REV X

MODEL 4500 | CODE | SHEET 4 OF 9

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
73					2	2	3050-1007	RESISTOR	R44, 80		1Ω, 1/2W, 5%	
74					1	1	3050-6806	"	R84		68Ω 1/2W, 5%	
75					1	1	3050-1000		R75		100Ω 1/2W, 5%	
76					2	2	3050-3900		R66, 76		390Ω, 1/2W, 5%	
77					1	1	3070-3900		R65		390Ω, 1 W, 5%	
78					1	1	3200-0003		R83		0.5Ω, 3W 5%	
79					1	1	3000-2203		R61		220K, 1/4W, 5%	
80					1	1	3000-1104	RESISTOR	R46		1.1M, 1/4W, 5%	
81					2	2	3300-0089	TRIM POT	R9, 12		100Ω	
82												
83					1	1	3300-0054-10	TRIM POT	R11		5K	
84					2	2	-0095		R1, 2		20K	
85					2	2	-0084		R5, 10		50K	
86					5	5	-0085		R3, 4, 6, 7, 8		100K	
87					1	1	3300-0088	TRIM POT	R13		1M	
88					-	24	4000-0005	CAPACITOR	24, 29, 54-74, 78		.01uf, 100V	
89					4	4	4000-0043	CAPACITOR	C25, 34, 35, 36		.01uf, 500V	
90					1	1	4010-0102	CAPACITOR	C7		.001uf, 100V	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO. | NUMBER | QTY | NEXT ASSEMBLY

LIST OF MATERIAL
CRT DRIVER

biomation

B | 0285-0050 | REV X

MODEL 4500 | CODE | SHEET 5 OF 9

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
91					11	11	4000-0009	CAPACITOR	C38, 13, 14, 17, 18, 21, 27, 43, 49, 77		.1uf, 100V	
92					1	1	4300-0036		C33		2.2uf, 20V	
93					2	2	4000-0042		C19, 42		.15uf, 100V	
94					5	5	4000-0007		C9, 40, 50, 6, 12		1uf, 50V	
95					1	1	4200-0037-30		C46		.01uf, 400V	
96					1	1	4200-0045-10		C45		.015uf, 400V	
97					2	2	4200-0040		C37, 38		.047uf, 100V	
98					1	1	4300-0043		C32		.0033uf, 80V	
99					3	3	4300-0038		C4, 31, 39		.0047uf, 80V	
100					1	1	4200-0010		C51		.47uf, 100V	
101												
102					4	4	4400-0037		C15, 16, 22, 43		470uf, 25V	
103					1	1	4400-0036		C23		1000uf, 16V	
104					3	3	4300-0005		C20, 44, 76		10uf, 20V	
105					2	2	4200-0014		C2, C1		.0022uf, 100V	
106					1	1	4400-0038		C28		10uf, 100V	
107					1	1	4200-0030		C47		3uf, 50V, 2%	
108					2	2	4100-0024	CAPACITOR	C10, 52		68pf, 500V	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO | NUMBER | QTY | NEXT ASSEMBLY

LIST OF MATERIAL
CRT DRIVER

biomation

B | 0285-0050 | REV X

MODEL 4500 | CODE | SHEET 6 OF 9

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
109					1	1	4100-0011	CAPACITOR	C30		150pf, 500V	
110					1	1	4100-0014		C26		120pf, 500V	
111					1	1	4100-0002		C41		470pf, 500V	
112					1	1	4100-0015		C79		1000pf, 500V	
113					1	1	4100-0019	CAPACITOR	C53		50pf, 500V	
114												
115					1	1	6100-0190-10	SOCKET, CRT	P2		7 PIN	
116												
117					1	1	6100-0118	SOCKET, DIP	U7		8 PIN	
118												
119					2	2	7000-0041	HEATSINK	Q3,7		TO-5	
120					3	3	7000-0365	HEATSINK	U8,4, Q9		TO-220	
121					1	1	7000-0366	HEATSINK	U5			
122					1	1	6000-0298	CONNECTOR			3 PIN	
123					1	1	6000-0329	SHORT. PLUG	E1,2,3			
124					3	3	7200-0017	INSULATOR				
125					3	3	7000-0221	INS. WASHER				
126					2	2	7000-0120	EJECTOR				

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
CRT DRIVER

biomation

B | 0285-0050 | REV X

MODEL 4500 | CODE | SHEET 7 OF 9

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
127					8	–	1800-0340	IC	U21,23,25,27,29 31,33,35		EPROM (2764)	
128												
129					2	2	1800-0240		U13,37		74LS244	
130					2	2	-0193		U40,41		74LS138	
131					1	1	-0105		U42		74LS00	
132												
133					1	1	1800-0109	I.C.	U19		74LS08	
134					1	–	9000-0054	WIRE			FORMED	
135					8	8	6100-0122	SOCKET	U22,24,26,28 30,32,34,36		24 PIN	
36					8	8	6100-0151	SOCKET	U21,23,25,27 29,31,33,35		28 PIN	
137					1	1	6000-0359-06	HEADER	P1		6 PIN	
138					2	2	1800-0298	IC	U38,39		74LS373	
139					3	3	3700-0049	R-PAK	RP11,12,14		3K/6.2K 10 PIN SIP (8)	
140					3	3	3700-0067	R-PAK	RP13,15,16		100Ω 10 PIN SIP (5)	
141					1	1	3700-0075	R-PAK	RP10		4.7K 10 PIN SIP (9)	
142												
143					–	1	0285-0374-01	PROM I.C.	U21			
144					–	1	0285-0374-02	PROM I.C.	U22			

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
CRT DRIVER

biomation

B | 0285-0050 | REV X

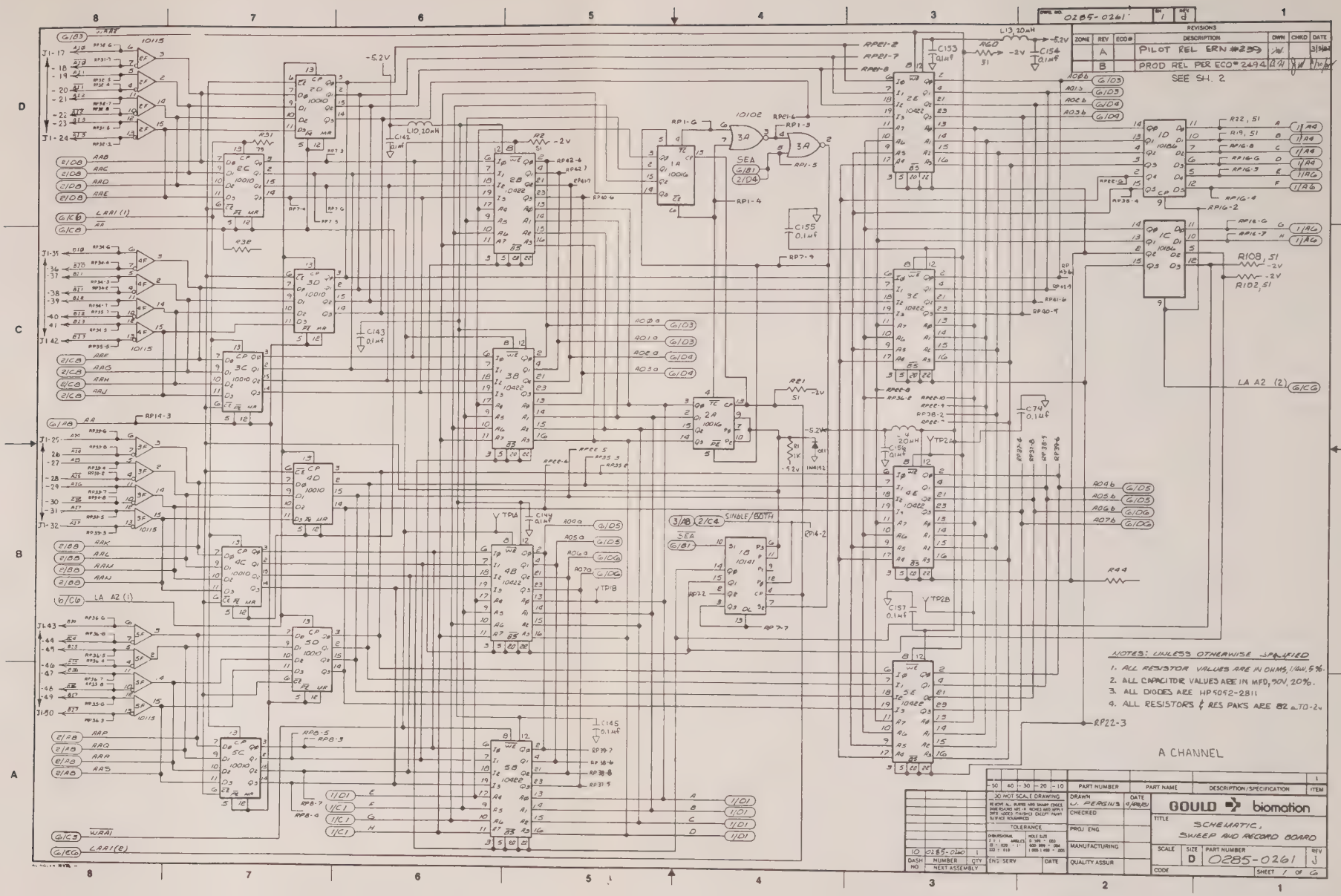
MODEL 4500 | CODE | SHEET 8 OF 9

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
145								-	1	0285-0374-03	PROM IC	U23	
146								-	1	-04		U24	
147								-	1	-05		U25	
148								-	1	-06		U26	
149								-	1	-07		U27	
150								-	1	-08		U28	
151								-	1	-09		U29	
152								-	1	-10		U30	
153								-	1	-11		U31	
154								-	1	-12		U32	
155								-	1	-13		U33	
156								-	1	-14		U34	
157								-	1	-15		U35	
158								-	1	0285-0374-16	PROM IC	U36	
159								3	3	7011-1440-12	SCREW, X, 4-40 X .375		
160								5	5	7071-1440-00	NUT & LOCK WASHER ASSY		

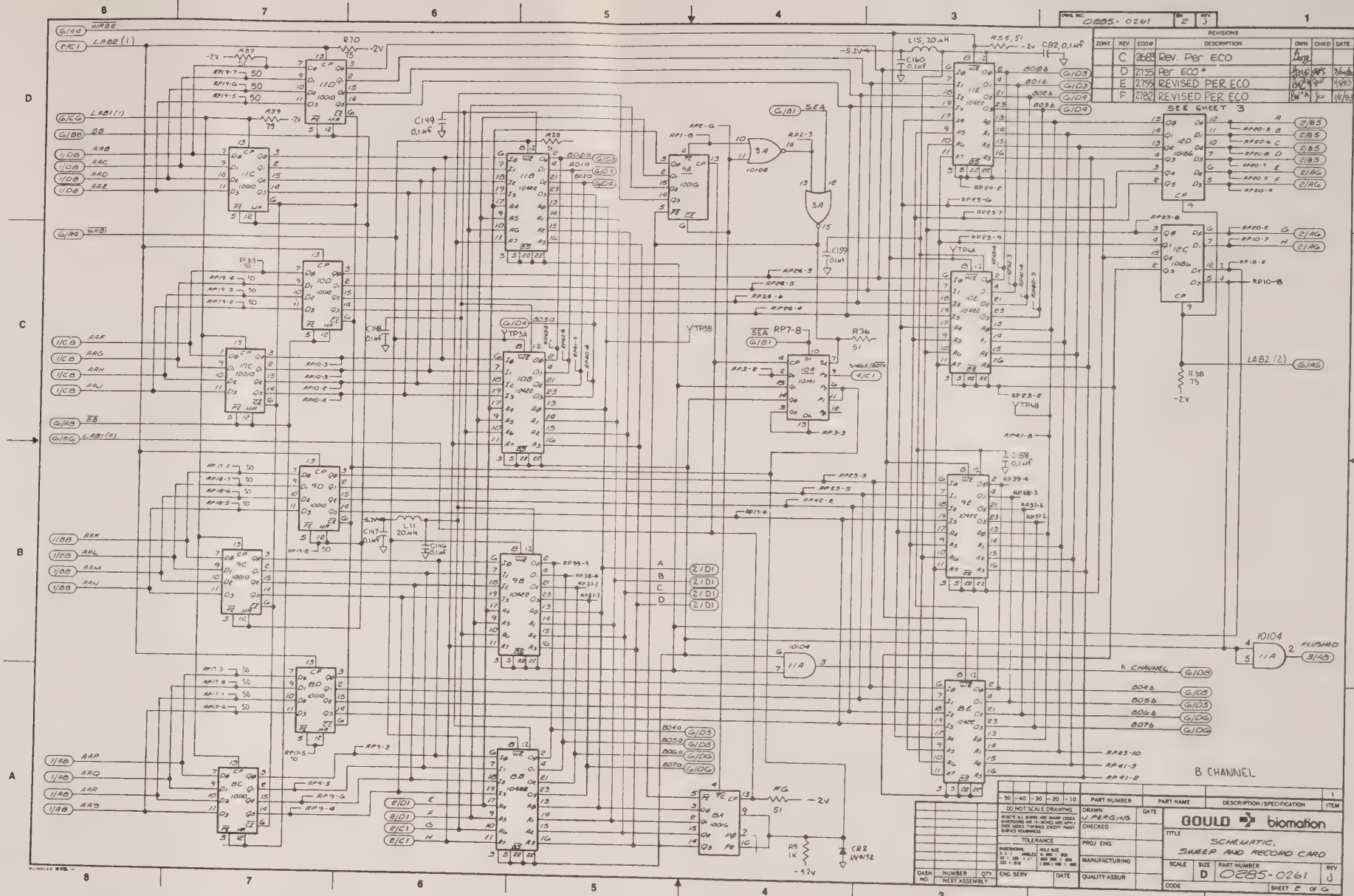
NOTES

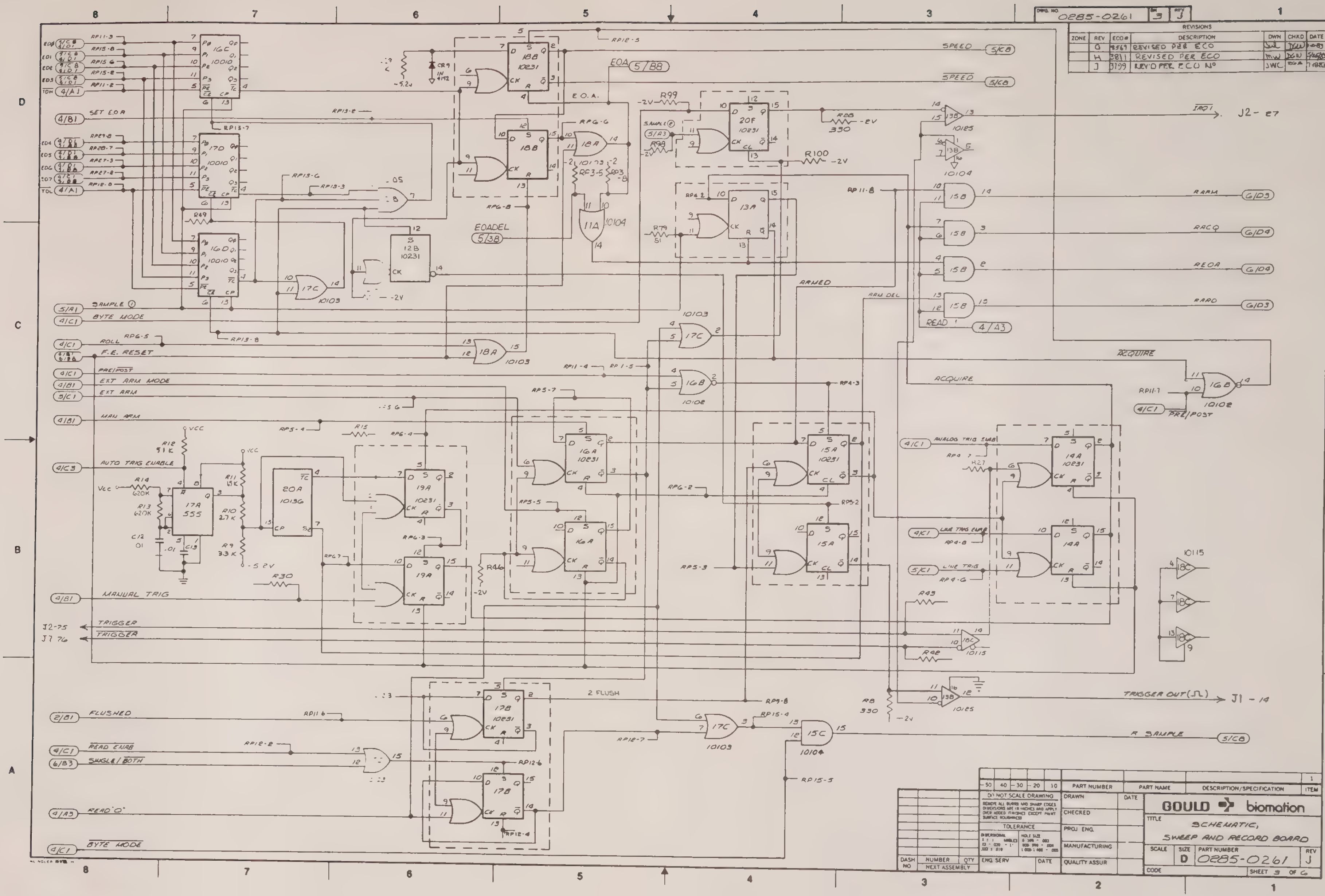
LIST OF MATERIAL
CRT DRIVER

GOULD ⇒ biomation
B 0235-0050 REV X
MODEL 4500 SHEET 2 OF 9

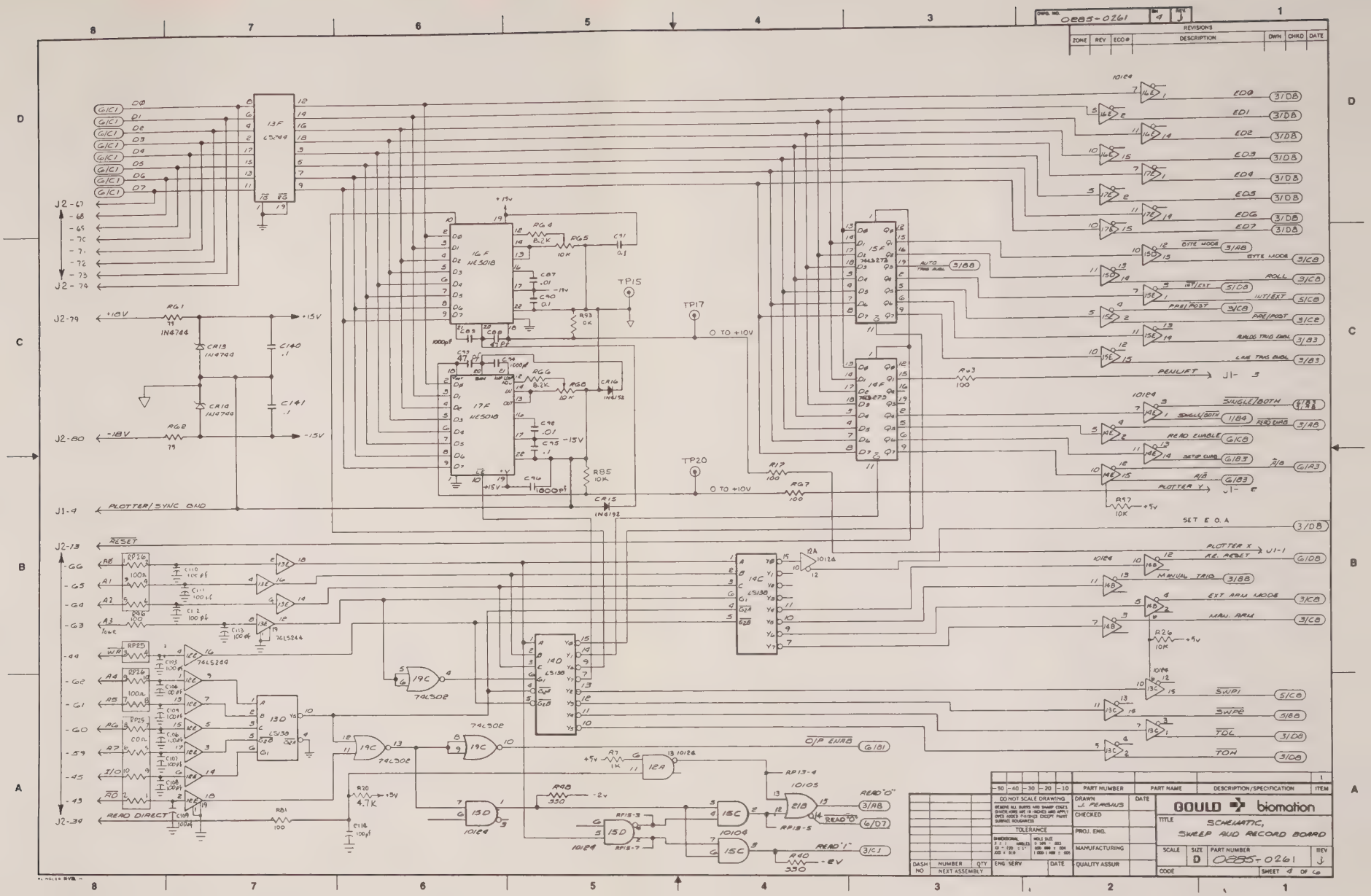


DWG. NO. 0285-0261
SH. 1
REV. d
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
A | PILOT REL ERN #239
B | PROD REL PER ECO# 2494
SEE SH. 2
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITOR VALUES ARE IN MFD, 50V, 20%.
3. ALL DIODES ARE HP5052-2811
4. ALL RESISTORS & RES PAKS ARE 82 a TO -2v
A CHANNEL
DO NOT SCALE DRAWING
TOLERANCE
DRAWN J. PERGINS
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE SCHEMATIC, SWEEP AND RECORD BOARD
SCALE
SIZE D
PART NUMBER 0285-0261
REV J
CODE
SHEET 1 OF 6
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
10 0285-0260 1

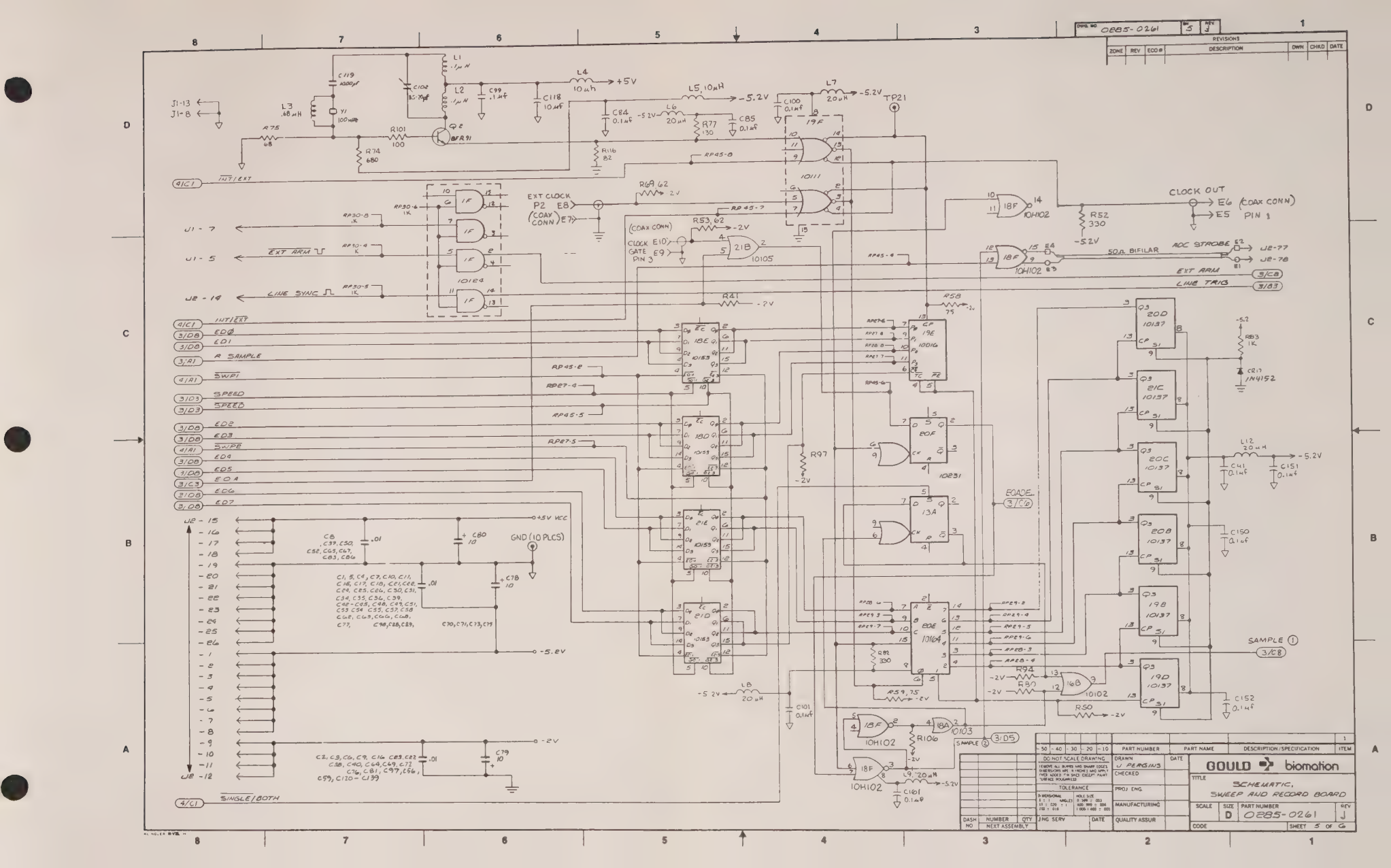

0285-0261
REVISIONS
C 2685 Rev. Per ECO
D 2735 Per ECO*
E 2795 REVISED PER ECO
F 2782 REVISED PER ECO
SEE SHEET 3
B CHANNEL
A CHANNEL
LAB2 (2)
SCHEMATIC,
SWEEP AND RECORD CARD
GOULD biomation
0285-0261

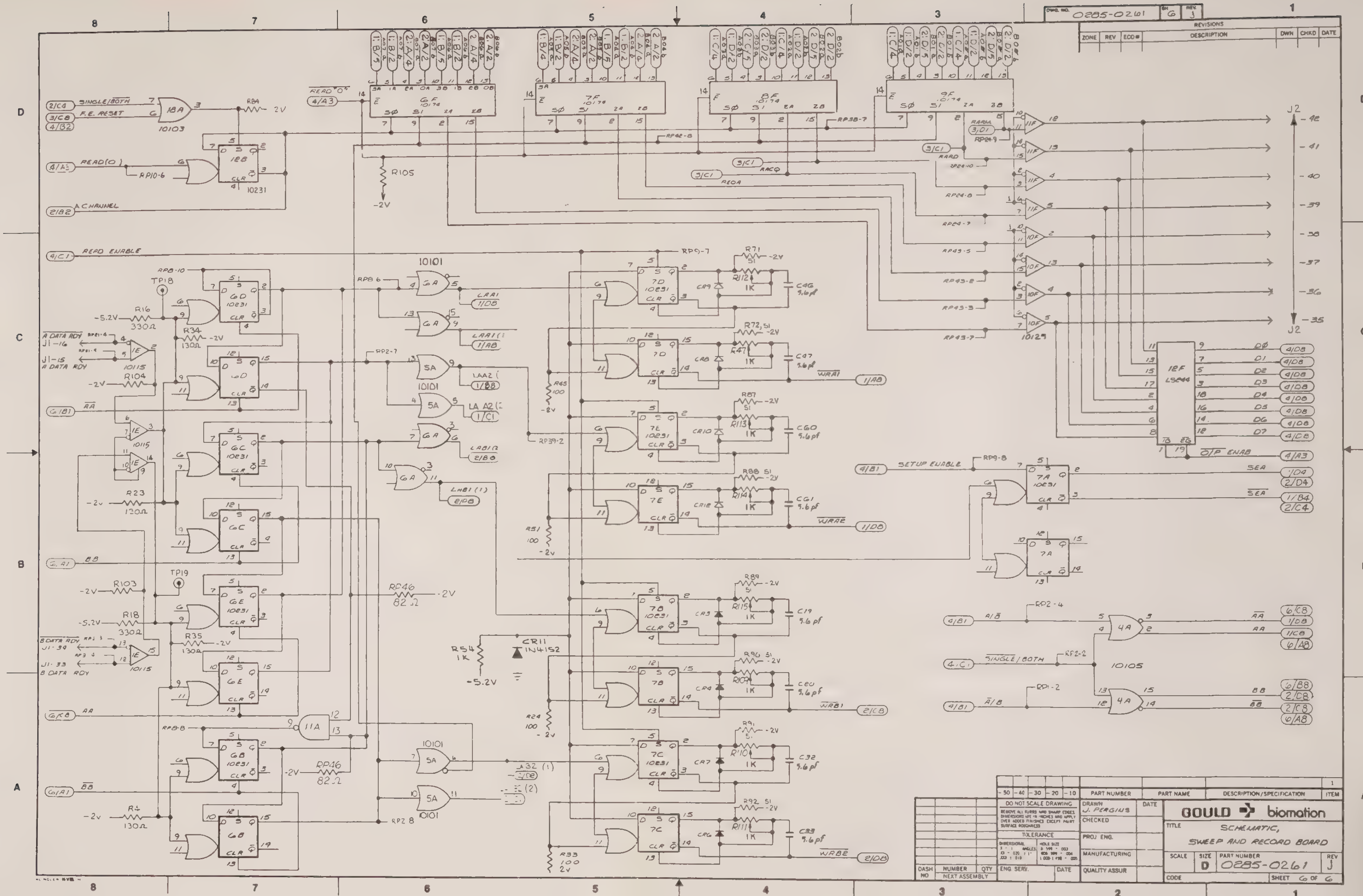


0285-0261
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
G | REVISED PER ECO
H | 2811 | REVISED PER ECO
J | 3199 | REV'D PER ECO No
SPEED 5/C8
SPEED 5/C8
EOA 5/B8
E.O.A.
SET E.O.A
IRQ1 J2-e7
RARM G/D3
RACQ G/D4
REOA G/D4
RARD G/D3
READ 4/A3
ARMED
ARM DEL
EOADEL 5/38
SAMPLE
BYTE MODE
ROLL
F.E. RESET
PRE/POST
EXT ARM MODE
EXT ARM
MAN ARM
AUTO TRIG ENABLE
MANUAL TRIG
TRIGGER
TRIGGER
J2-75
J7 76
ACQUIRE
ACQUIRE
ANALOG TRIG ENAB
LINE TRIG ENAB
LINE TRIG
FLUSHED
2 FLUSH
READ ENAB
SINGLE/BOTH
READ "0"
BYTE MODE
TRIGGER OUT J1-14
R SAMPLE 5/C8
17A 555
20A 10136
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
SCHEMATIC, SWEEP AND RECORD BOARD
SCALE
SIZE D
PART NUMBER 0285-0261
REV J
CODE
SHEET 3 OF 6



0285-0261
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
13F
LS244
16F
NE5018
17F
NE5018
15F
74LS273
14F
74LS273
14C
LS138
14D
LS138
13D
LS138
13C
74LS244
74LS02
TP15
TP17
TP20
0 TO +10V
J2-67
J2-68
J2-69
J2-70
J2-71
J2-72
J2-73
J2-74
J2-79
J2-80
J1-4
J2-13
J2-34
+18V
-18V
+15V
-15V
PLOTTER/SYNC GND
RESET
READ DIRECT
ED0
ED1
ED2
ED3
ED4
ED5
ED6
ED7
BYTE MODE
ROLL
INT/EXT
PRE/POST
ANALOG TRIG ENBL
LINE TRIG ENBL
PENLIFT
SINGLE/BOTH
READ ENABLE
SETUP ENAB
PLOTTER Y
SET E.O.A
PLOTTER X
F.E. RESET
MANUAL TRIG
EXT ARM MODE
MAN. ARM
SWP1
SWP2
TOL
TOH
O/P ENAB
READ "0"
READ "1"
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
J. PERGINS
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE
SCHEMATIC,
SWEEP AND RECORD BOARD
SCALE
SIZE
D
PART NUMBER
0285-0261
REV
CODE
SHEET 4 OF 6


DWG NO 0285-0261
REV J
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
J1-13
J1-8
L1 .1μH
L2 .1μH
C119 1000pf
C102 5-70pf
Y1 100 MHz
L3 .68μH
Q2 BFR91
A75 68
R101 100
R74 680
C99 .1μf
C118 10μf
L4 10μh +5V
L5 10μH -5.2V
C84 0.1μf -5.2V
L6 20μH
R77 130
C85 0.1μf
R116 82
C100 0.1μf
L7 20μH -5.2V
TP21
19F
10111
RP45-8
RP45-7
R69 62 2V
EXT CLOCK P2 E8 (COAX CONN) E7
(COAX CONN) CLOCK E10 GATE E9 PIN 3
R53 62 -2V
21B 10105
CLOCK OUT
E6 (COAX CONN)
E5 PIN 1
R52 330 -5.2V
18F 10H102
50Ω BIFILAR
ADC STROBE E2
J2-77
J2-78
EXT ARM 5/C8
LINE TRIG 3/B3
U1-7
U1-5 EXT ARM
U2-14 LINE SYNC
RP30-6 1K
RP30-8 1K
RP30-4 1K
RP30-5 1K
10124
R41 -2V
R58 75 -2V
4/C1 INT/EXT
3/D8 ED0
3/D8 ED1
3/A1 A SAMPLE
4/A1 SWP1
3/D3 SPEED
3/D3 SPEED
3/D8 ED2
3/D8 ED3
4/A1 SWPE
3/D8 ED4
3/D8 ED5
3/C3 EOA
2/D8 ED6
3/D8 ED7
18E 10153
19E 10016
Q3 20D 10137
Q3 21C 10137
Q3 20C 10137
Q3 20B 10137
Q3 19B 10137
Q3 19D 10137
18C 10231
13A
20A 10164
R97 -2V
R91 330
R94 -2V
R90 -2V
R59 75 -2V
16B 10102
R50 -2V
EOADE 3/C6
SAMPLE 1 3/C8
L12 20μH -5.2V
C141 0.1μf
C151 0.1μf
C150 0.1μf
C152 0.1μf
RB3 1K -5.2
CR17 1N4152
L8 20μH -5.2V
C101 0.1μf
L9 20μH -5.2V
C101 0.1μf
18F 10H102
18A 10103
R106 -2V
SAMPLE 2 3/D5
J2-15 +5V VCC
J2-16
J2-17
J2-18
J2-19
J2-20
J2-21
J2-22
J2-23
J2-24
J2-25
J2-26
J2-1
J2-2
J2-3
J2-4
J2-5
J2-6
J2-7
J2-8
J2-9
J2-10
J2-11
J2-12 -2V
C8, C39, C50, C52, C63, C67, C83, C86 .01
C80 10 GND (10 PLCS)
C1, 3, C4, C7, C10, C11, C16, C17, C18, C21, C22, C24, C25, C26, C30, C31, C34, C35, C36, C39, C42-C45, C48, C49, C51, C53 C54 C55, C57, C58 C68, C69, C46, C66, C68, C77, C90, C28, C89, C70, C71, C73, C75 .01
C78 10
C2, C3, C6, C9, C14 C83, C82 C38, C40, C64, C69, C72 C76, C81, C97, C96, C59, C120-C139 .01
C79 10
4/C1 SINGLE/BOTH
DO NOT SCALE DRAWING
TOLERANCE
DRAWN J. PERGINS
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC, SWEEP AND RECORD BOARD
SCALE D
PART NUMBER 0285-0261
REV J
CODE
SHEET 5 OF 6

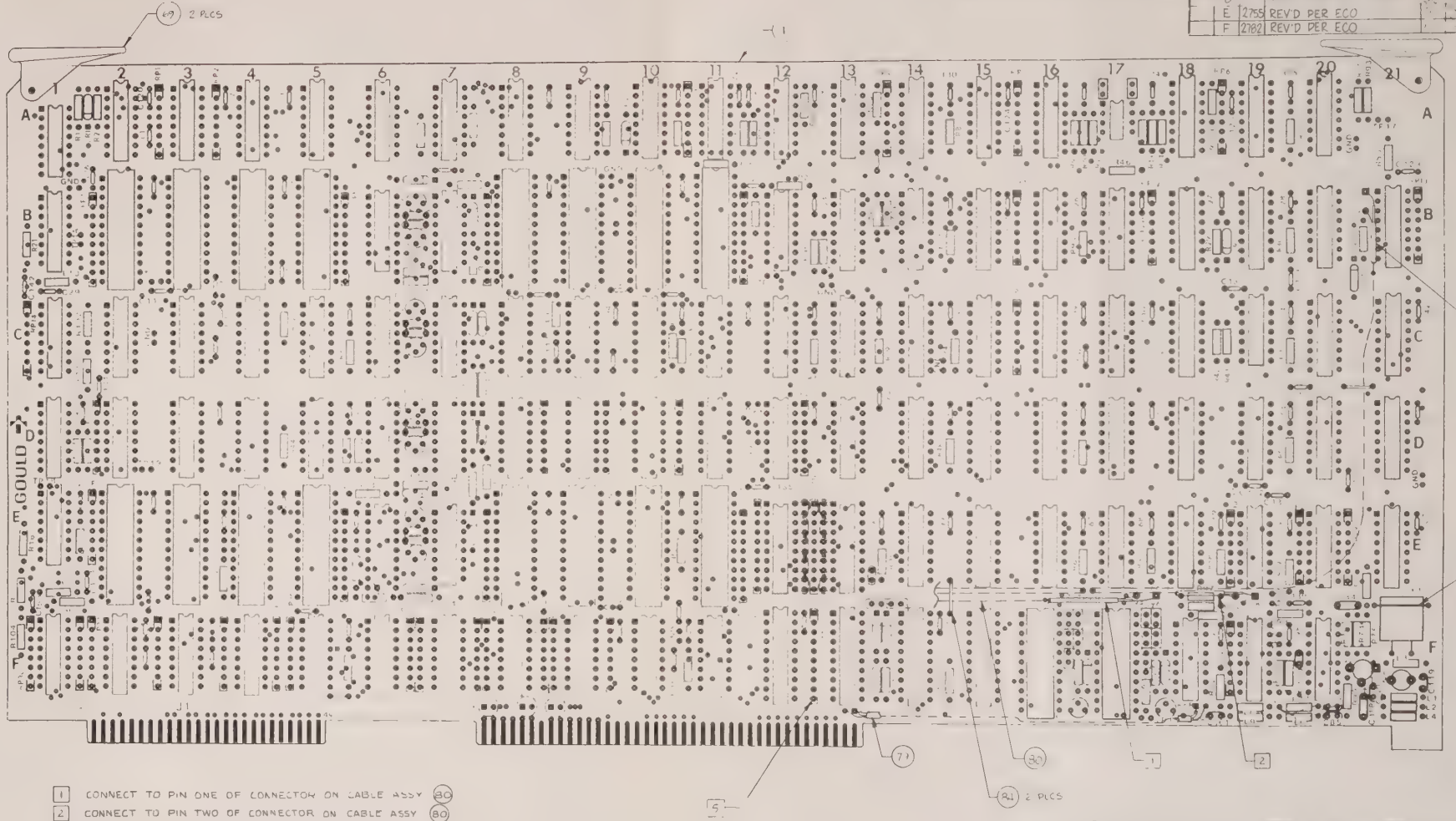

DWG. NO. 0285-0261 SH 6 REV J
REVISIONS
ZONE
REV
ECO #
DESCRIPTION
DWN
CHKD
DATE
DO NOT SCALE DRAWING
TOLERANCE
DRAWN J. PERGINS
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV.
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE SCHEMATIC, SWEEP AND RECORD BOARD
SCALE
SIZE D
PART NUMBER 0285-0261
REV J
CODE
SHEET 6 OF 6

REV	ECO	DESCRIPTION	DWN	CHKD	DATE
G	3569	REVISED PER ECO	[illegible]	DGW	10 83
H	3811	REVISED PER ECO	[illegible]	[illegible]	[illegible]
J	3749	REV'D PER ECO	[illegible]	[illegible]	[illegible]

DWG NO 0285-0260

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL ERN 239			
	B		[illegible]			
	C		REV'D PER [illegible]	[illegible]	[illegible]	[illegible]
	D		[illegible]			
	E	2755	REV'D PER ECO			
	F	2782	REV'D PER ECO			



1. CONNECT TO PIN ONE OF CONNECTOR ON CABLE ASSY 80
2. CONNECT TO PIN TWO OF CONNECTOR ON CABLE ASSY 80
3. CONNECT TO PIN THREE OF CONNECTOR ON CABLE ASSY 80
4. TIE DOWN CRYSTAL
5. RP44 IS NOT INSTALLED.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY ONLY ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES; XX ± .020 1; XXX ± .010 ; HOLE SIZE: 0-.599 .003; 600-.999 .004; 1.000-1.499 .005

DRAWN [illegible] DATE 11-30-81

CHECKED

PROJ ENG

MANUFACTURING

QUALITY ASSUR

ENG SERV DATE

GOULD biomation

TITLE ASSEMBLY SWEEP & RECORD

SCALE 2/1 SIZE D PART NUMBER 0285-0260 REV J

CODE 4500 SHEET 1 OF 1

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0285-0262	PCB, FAB				-M
2						REF	0285-0261	SCHEMATIC				
3						2	1850-0037	IC	6A, 5A		10101	
4						19	1850-0083		2C, 2D, 3C, 3D, 4C, 8D, 9C, 9D, 10C, 10D, 11C, 4D, 5C, 5D, 6C, 11D, 14C, 16D, 17D		10010	
5						5	1850-0055		1A, 2A, 8A, 9A, 19E		10016	
6						2	1850-0002		3A, 16B		10102	
7						2	1850-0049		17C, 18A		10103	
8						3	1850-0057		11A, 15B, 15C		10104	
9						2	1850-0003		4A, 21B		10105	
10						1	1850-0029		19F		10111	
11						6	1850-0059		1E, 2F, 3F, 4F, 5F, 18C		10115	
12						9	1850-0021		1F, 13C, 14B, 15D, 15E, 16E, 17E, 14B, 12A		10124	
13						3	1850-0074		13B, 10F, 11F		10125	
14						1	1850-0083		20A		10136	
15						6	1850-0061		19B, 19D, 20B, 20C, 20D, 21C		10137	
16						2	1850-0053		1B, 10A		10141	
17						4	1850-0054		18D, 18E, 21D, 21E		10153	
18						1	1850-0042	I.C.	20E		10164	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL PER ERN 239	7/24/80			
B	PROD. REL PER ECO # 2494	5/4/82	B.H.		
C	REV'D PER ECO # 2683	7/30/82			
D	REV'D PER ECO # 2135	8/18/82			
E	REVISED PER ECO # 2755	11-29-82			
F	REVISED PER ECO # 2782	1-19-83			
G	REVISED PER ECO # 3569	6-10-83			

DASH NO.	NUMBER	QTY
-10	0285-0002	1
NEXT ASSEMBLY		

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL

P.C.B. ASSEMBLY, SWEEP & RECORD

biomation

B | 0285-0260 | REV K

MODEL 4500 | CODE | SHEET 1 OF 5

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19						4	1850-0090	I.C.	6F, 7F, 8F, 9F		10174	
20						4	1850-0073		1C, 1D, 12C, 12D		10186	
21						13	1850-0019		6B, 6C, 6D, 6E, 7A, 12B, 13A, 19A, 15A, 16A, 17B, 10B, 19A		10231	
22						16	1850-0088		2B, 2E, 3B, 3E, 4B, 8E, 9B, 9E, 10B, 4E, 5B, 5E, 6B, 10E, 11B, 11E		10422	
23						1	1700-0078		17A		555	
24						4	1800-0240		12E, 12F, 13E, 13F		74LS244	
25						2	1800-0231		14F, 15F		74LS273	
26						3	1800-0193		13D, 14C, 14D		74LS138	
27						1	1800-0106		19C		74LS02	
28												
29						2	1900-0013		16F, 17F		NE5018	
30						1	1850-0022		7.5A		10107	
31						5	1850-0075	I.C.	7B, 7C, 7D, 7E, 20F		10231 (MOTOROLA ONLY)	
32						1	3000-1300	RESISTOR	R77		130Ω, 1/4W, 5%	
33						1	1900-0038	TRANSISTOR	Q8		BFR 91	
34						7	1000-0002	DIODE	CR1, 2, 9, 11, 13, 16, 17		IN4152	
35						2	1100-0027	DIODE	CR 13, 14		IN4744	
36						8	1000-0003	DIODE	CR 3, 4, 6-10, 12		HP5082-2811	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
H	REV'D PER ECO 3811	5/2/83	MW	DGW	
I	REV'D PER ECO 3799	7/7/83			
K	REV PER ECO 4181	11/4/83	J.G.		

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL

P.C.B. ASSEMBLY- SWEEP & RECORD

biomation

B | 0285-0260 | REV K

MODEL 4500 | CODE | SHEET 2 OF 5

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
37						2	2100-0014	INDUCTOR	L1, L2		.14H	
38						1	2100-0046	INDUCTOR	L3		.39 MH	
39						6	3000-3300	RESISTOR	R8,28,40,48, R52,82		330Ω, 1/4W, 5%	
40						6	3000-1001		R1,5,7,29,54,83		1K	
41						1	3000-3301		R9		33K	
42						1	3000-2701		R10		2.7K	
43						1	3000-1501		R11		1.5K	
44						1	3000-6800		R74		680Ω 1/4W 5%	
45						1	3000-5101		R12		5.1K	
46						9	3000-7506		R31,38,39, 58,59,61,62,70,117		75Ω	
47						28	3000-8206		R4,15,23,27,30,32,34,35,41TO44,46,49,50 80,84,94,95,97,98,99,100,103TO106,116		82Ω	
48						10	3000-1000		R13,24,33,43,53,63, 68,81,96,101		100Ω	
49						4	3000-1002		R26,57,85,93		10K	
50						1	3000-6806		R75		68Ω	
51						2	3000-6203	RESISTOR	R13,14		620K, 1/4W, 5%	
52						2	3300-0031	RESISTOR, VAR.	R67,68		10K	
53						8	3300-0001	RESISTOR, VAR.	R47, R109-115		1K	
54						2	3000-8201	RESISTOR	R64,66		8.2K 1/4W 5%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

			DRAWN	DATE
			CHECKED	
			ENGINEER	
			MANUFACTURING	
			QUALITY ASSURANCE	
DASH NO.	NUMBER NEXT ASSEMBLY	QTY		

LIST OF MATERIAL

P.C.B ASSEMBLY, SWEEP & RECORD

biomation

B | 0285-0260 | REV K

MODEL 4500 | CODE | SHEET 3 OF 5

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
55												
56						32	3700-0025	RESISTOR PAK	RP1-6,11-16,20,21,27-29 31-43,45,46		82Ω 8PIN	
57						7	3700-0086	RESISTOR PAK	RP7-10,22-24		82Ω 10PIN	
58						91	4000-0033	CAPACITOR	C1-18 C21-31,34-40,42-45,48-59 62-73,75-77,81,83,86,87,98,120-125,127-129		.01UF, 50V, 20%	
59												
60												
61						4	4010-0102-10		C89,94,96,119		1000PF, 200V, 5%	
62						24	4000-0025		C41,74,82,84, 90,142-160		.1UF, 50V, 20%	
63						2	4010-0470		C88, C93		47PF, 100V, 5%	
64						9	4010-0104		C85,91,95,99-101,140,141,161		0.1UF, 100V, 10%	
65						4	4300-0013	CAPACITOR	C78-80,118		10MF, 10V, 10%	
66						2	4010-0103	CAP	C87,92		.01uf 50V 10%	
67						1	4600-0011	CAP. VAR	C102		3.5-20 PF	
68						1	5100-0004	CRYSTAL	Y1		100MHz	
69						2	7000-0120	EJECTOR, CARD				
70						8	4010-5606	CAP	C1,2,20,38,33,44,47,48, 51		5.6 PF, 100V. 5%	
71						21	3000-5106	RES.	R2,6,19,21,22,25,34,37,55,60,71,72 79,87-92,102,108		51Ω 1/4W, 5%	
72						3	3700-0038	R. PACK	RP17,18,19		50Ω 0.3W 2%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

			DRAWN	DATE
			CHECKED	
			ENGINEER	
			MANUFACTURING	
			QUALITY ASSURANCE	
DASH NO.	NUMBER NEXT ASSEMBLY	QTY		

LIST OF MATERIAL

P.C.B. ASSEMBLY, SWEEP & RECORD

biomation

B | 0285-0260 | REV K

MODEL 4500 | CODE | SHEET 4 OF 5

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
73						12	4010-0101	CAP	C103-114		100 pf 500V	
74						2	3700-0067	R. PACK	RP 25, 26		100 Ω, 5 RES	
75												
76						2	3000-6206	RES	R53, 69		62 Ω 1/4W 5%	
77												
78						1	3700-0016	R PACK	RP30		1K BAN	
79						A/R	9000-0116	BIFILAR			50 OHM	
80						1	0285-0332	CABLE ASSY				
81						25	0285-0311	TEST POINT	TP1A, 1B, 2A, 2B, 3A, 3B 4A, 4B, TP5-21			
82						2	2100-0007	INDUCTOR	L4, 5		10μH	
83						10	2100-0036-20	INDUCTOR	L6 THRU L15		20μH	
84						2	7200-0025	MOUSE TAIL				
85						A/R	7100-0099	WIRE				
86						1	1850-0132	I.C.	18 f		10H102	
87						1	3000-4701	RES.	R20		4.7K 1/4W 5%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	G Galindo	11-17-81
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

P.C.B ASSEMBLY
SWEEP & RECORD

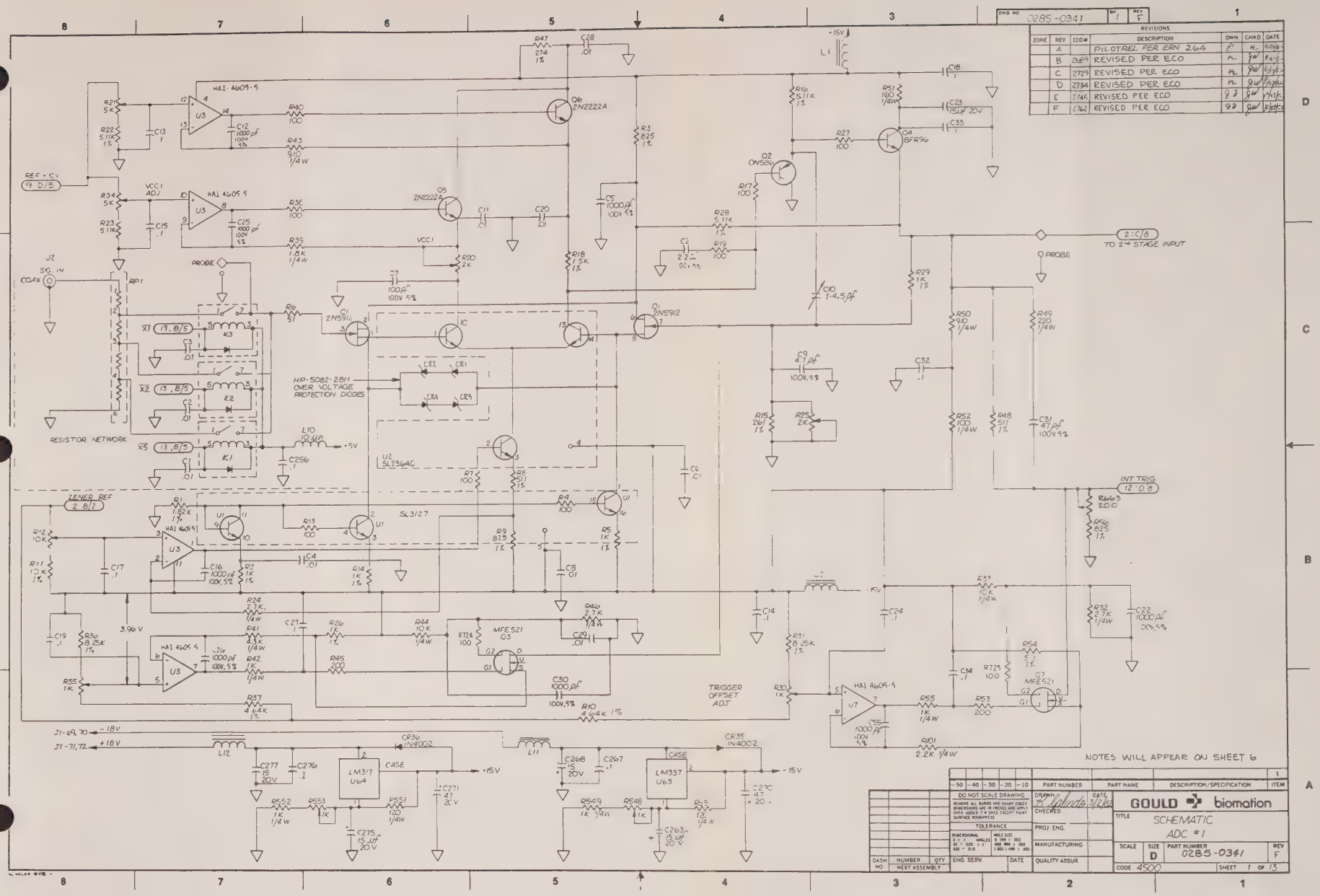
MODEL 4500

biomation

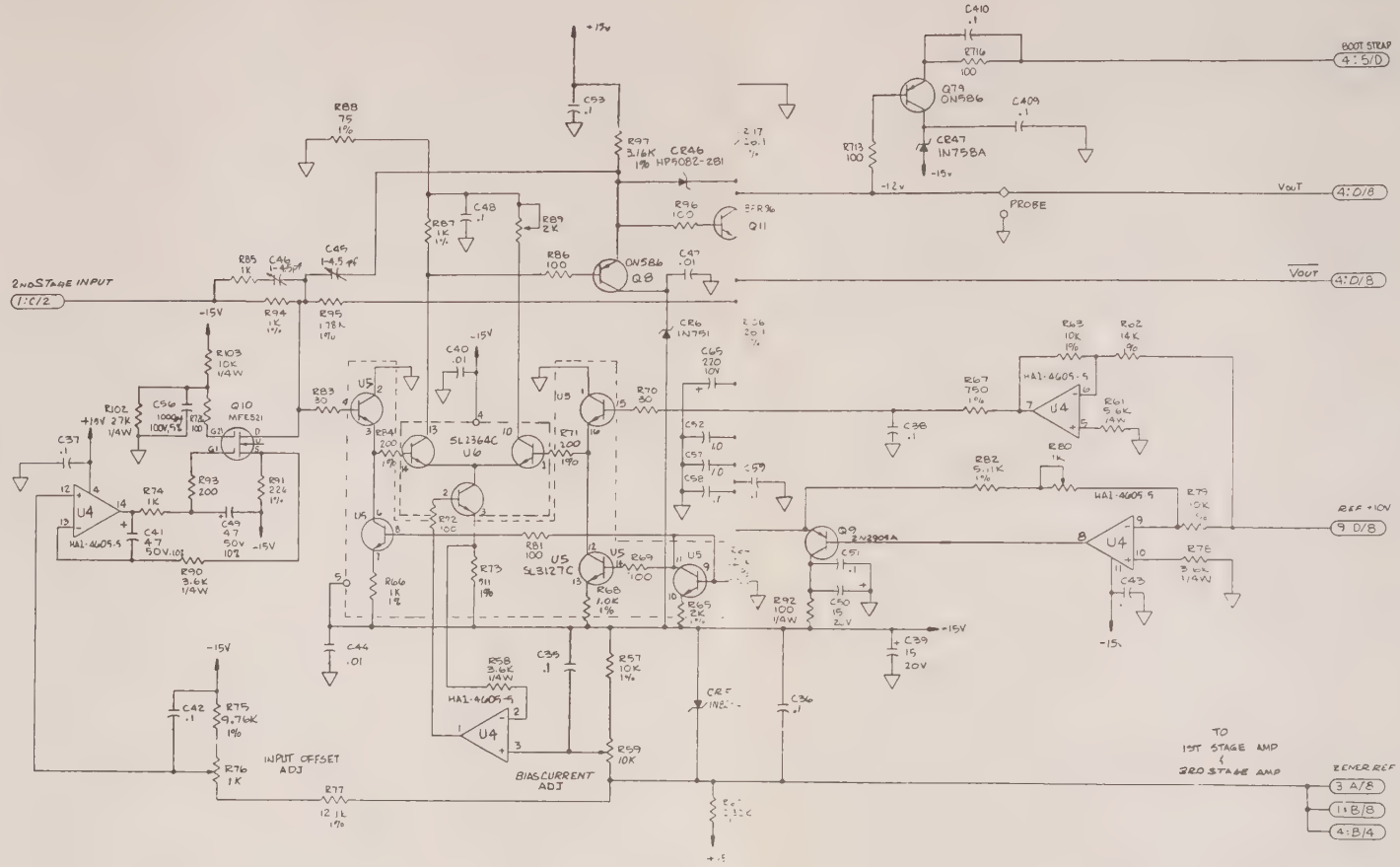
B | 0285-0260 | REV K

CODE

SHEET 5 OF 5



DWG NO 0285-0341
SH 1
REV F
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
A | PILOTREL PER ERN 264
B | 2689 | REVISED PER ECO
C | 2729 | REVISED PER ECO
D | 2734 | REVISED PER ECO
E | 2745 | REVISED PER ECO
F | 2762 | REVISED PER ECO
REF +10V 9 D/8
VCC1 ADJ
J2 SIG. IN COAX
RP1
RESISTOR NETWORK
PROBE
HP-5082-2811 OVER VOLTAGE PROTECTION DIODES
U2 SL2364C
ZENER REF 2 B/2
SL3127
TRIGGER OFFSET ADJ
2:C/8 TO 2nd STAGE INPUT
INT TRIG 12:D/8
J1-69,70 -18V
J1-71,72 +18V
LM317 U64
LM337 U63
CASE
NOTES WILL APPEAR ON SHEET 6
DO NOT SCALE DRAWING
TOLERANCE
DRAWN K. Galindo
DATE 3/2/83
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV.
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE SCHEMATIC ADC #1
SCALE
SIZE D
PART NUMBER 0285-0341
REV F
CODE 4500
SHEET 1 OF 13



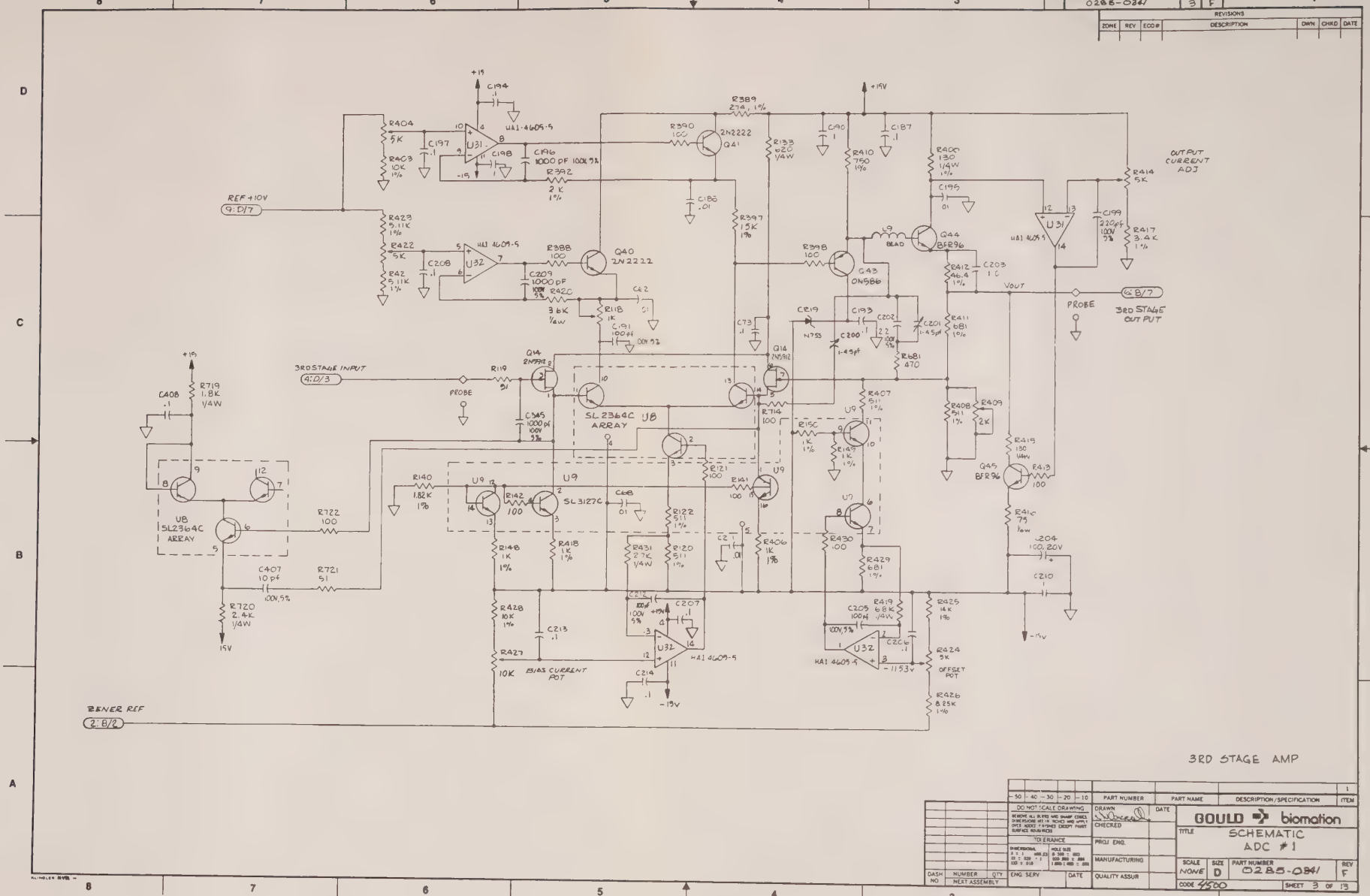
2ND STAGE AMP

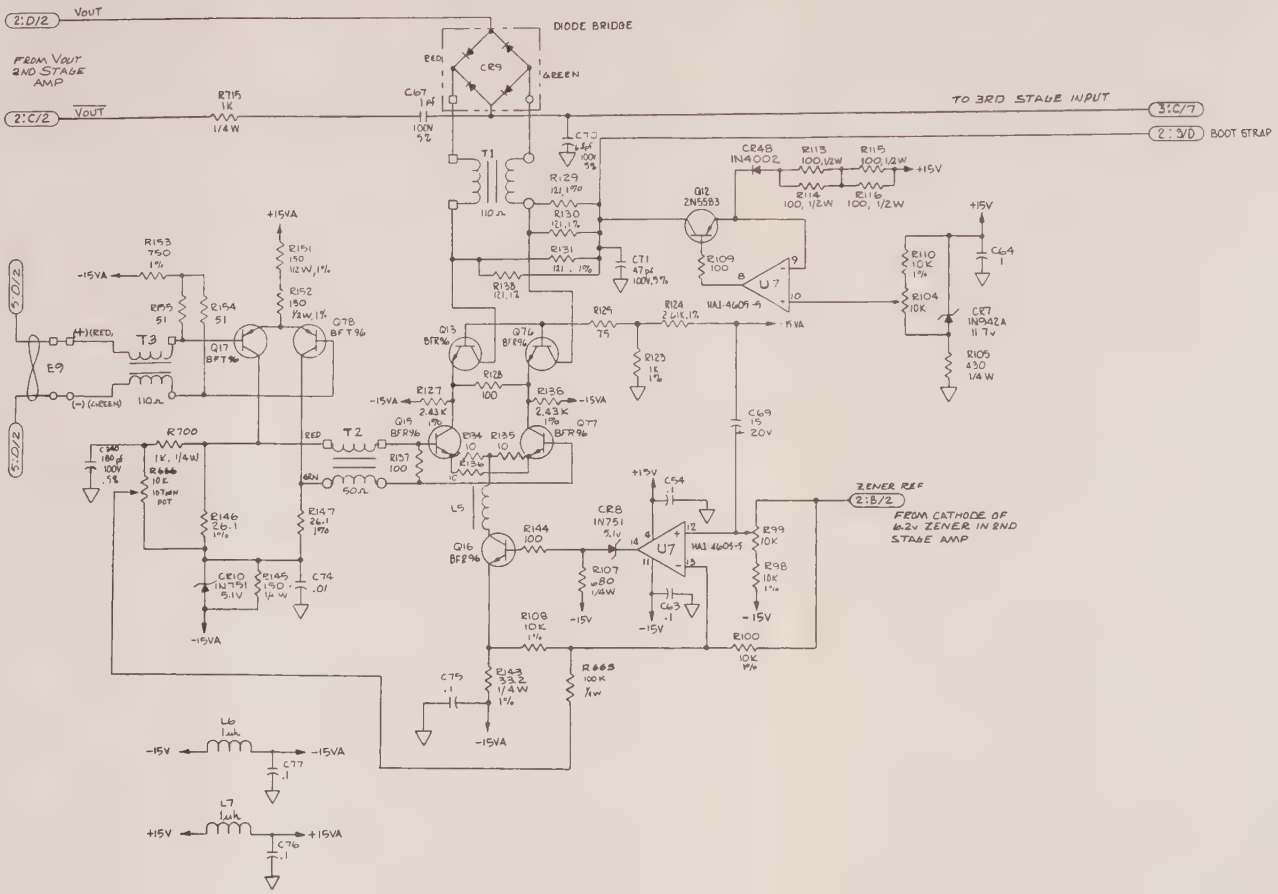
DWG. NO.	SIZE	REV
0285-0341	2	F

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING	DRAWN	DATE	GOULD biomation
TOLERANCE	CHECKED		TITLE SCHEMATIC ADC #1
	PROJ ENG.		
	MANUFACTURING		SCALE NONE · SIZE D · PART NUMBER 0285-0341 · REV F
ENG. SERV.	QUALITY ASSUR		CODE 45500 · SHEET 2 OF 13


DWG. NO. 0285-0341
REV F
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
REF +10V
9:D/7
3RD STAGE INPUT
4:D/3
PROBE
OUTPUT CURRENT ADJ
VOUT
PROBE
3RD STAGE OUT PUT
@B/7
SL2364C UB ARRAY
UB SL2364C ARRAY
SL3127C
HA1 4609-5
2N2222
BFR96
ON586
N753
BEAD
BIAS CURRENT POT
OFFSET POT
ZENER REF
2:B/2
3RD STAGE AMP
GOULD biomation
SCHEMATIC
ADC #1
PART NUMBER 0285-0341
REV F
SCALE NONE
SIZE D
CODE 14500
SHEET 3 OF 13



DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ITEM	DESCRIPTION/SPECIFICATION	PART NAME	PART NUMBER
1			

DO NOT SCALE DRAWING

TOLERANCE

ENG. SERV | DRAWN | CHECKED | PROJ. ENG. | MANUFACTURING | QUALITY ASSUR | DATE

GOULD biomation

TITLE: SCHEMATIC ADC #1

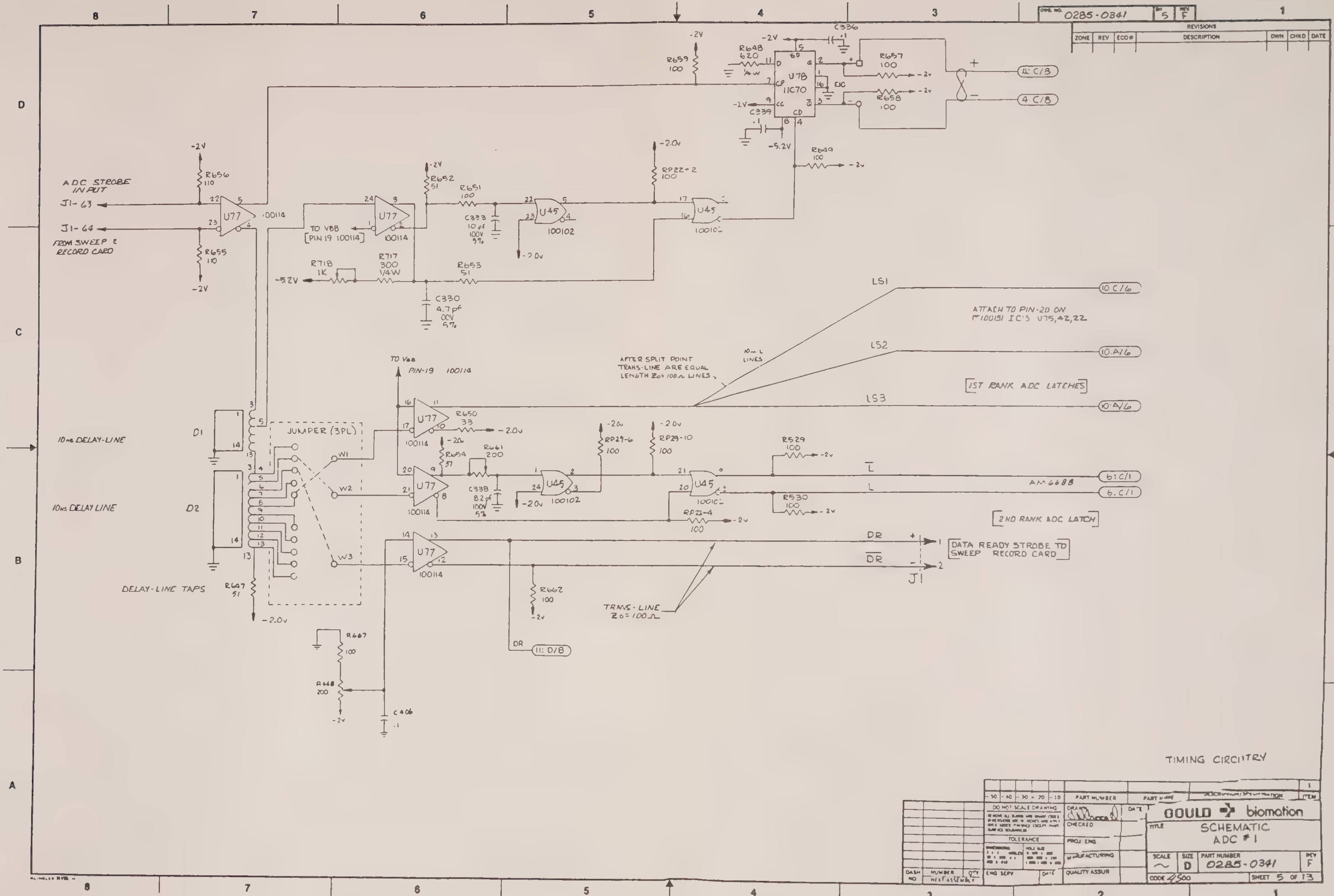
SCALE: | SIZE: D | PART NUMBER: 0285-0941 | REV: F

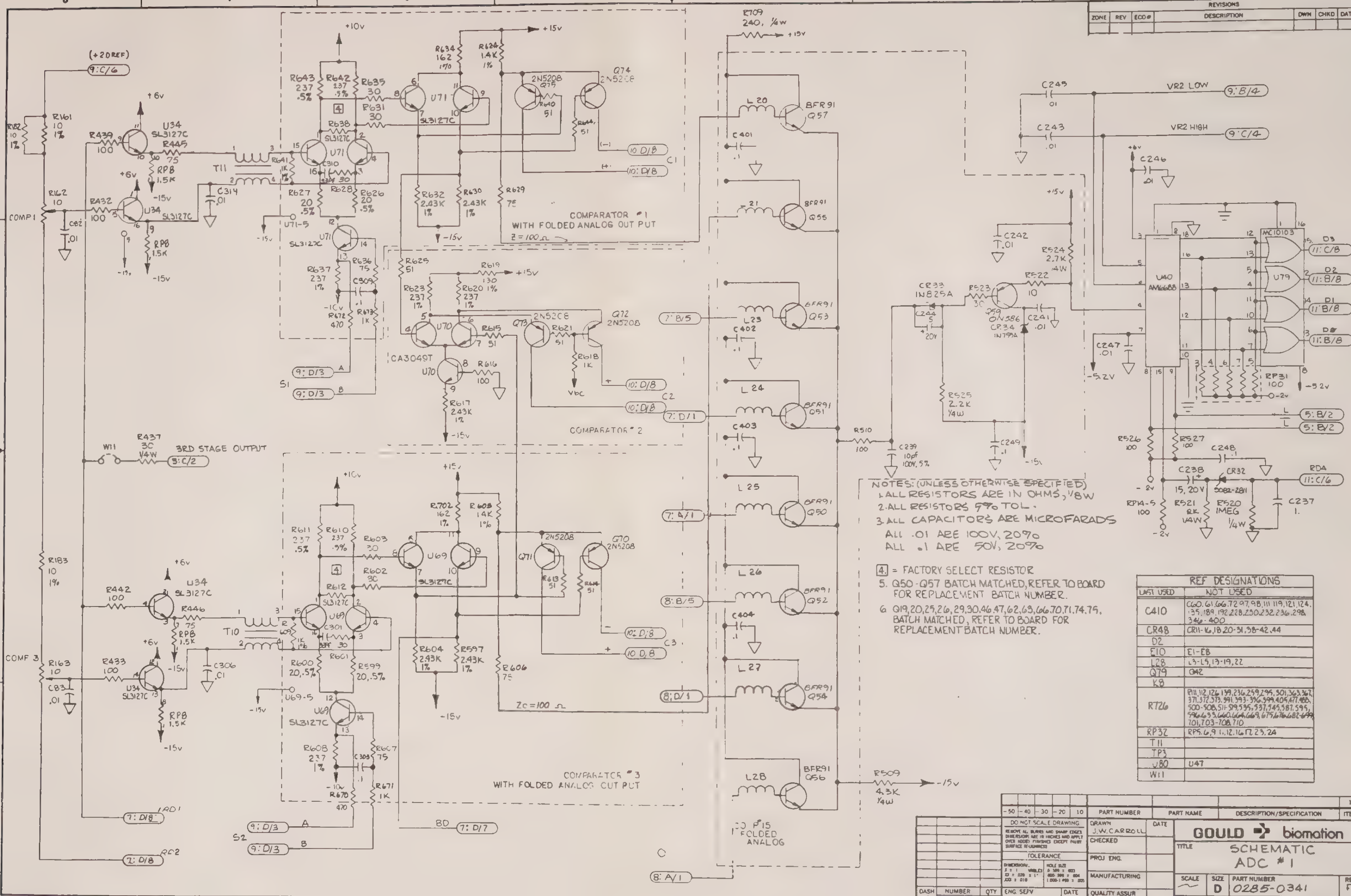
CODE 4500 | SHEET 4 OF 13

DWG. NO 0285-0341 | SH 4 | REV F

REVISIONS

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE


0285-0341
5
F
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
ADC STROBE INPUT
J1-63
J1-64
FROM SWEEP & RECORD CARD
R656 110
R655 110
-2V
U77
100114
TO VBB [PIN 19 100114]
R652 51
R651 100
C333 10pf 100V 5%
U45
100102
RP22-2 100
-2.0v
R718 1K
R717 300 1/4W
R653 51
-5.2V
C330 4.7pf 100V 5%
R659 100
R648 620 1/4W
U78 11C70
C336
C339 .1
-5.2V
R657 100
R658 100
R649 100
11 C/8
4 C/8
LS1
LS2
LS3
10 C/6
10 A/6
ATTACH TO PIN-20 ON 100151 IC'S U75,42,22
1ST RANK ADC LATCHES
AFTER SPLIT POINT TRANS-LINE ARE EQUAL LENGTH Zo=100Ω LINES
10ns DELAY-LINE
10ns DELAY LINE
D1
D2
JUMPER (3PL)
W1
W2
W3
TO Vbb PIN-19 100114
R650 33
R654 51
R661 200
C338 8.2pf 100V 5%
RP29-6 100
RP29-10 100
R529 100
R530 100
RP21-4 100
AM6688
6:C/1
6.C/1
2ND RANK ADC LATCH
DR
DATA READY STROBE TO SWEEP RECORD CARD
J1
R662 100
TRANS-LINE Zo=100Ω
11: D/8
DELAY-LINE TAPS
R647 51
-2.0v
R667 100
R668 200
C406 .1
TIMING CIRCUITRY
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
SCHEMATIC ADC #1
SCALE
SIZE D
PART NUMBER 0285-0341
REV F
CODE 4500
SHEET 5 OF 13



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE IN OHMS, 1/8W
2. ALL RESISTORS 5% TOL.
3. ALL CAPACITORS ARE MICROFARADS
   ALL .01 ARE 100V, 20%
   ALL .1 ARE 50V, 20%
4. (boxed) = FACTORY SELECT RESISTOR
5. Q50-Q57 BATCH MATCHED, REFER TO BOARD FOR REPLACEMENT BATCH NUMBER.
6. Q19,20,25,26,29,30,46,47,62,63,66,70,71,74,75, BATCH MATCHED, REFER TO BOARD FOR REPLACEMENT BATCH NUMBER.

REF DESIGNATIONS	
LAST USED	NOT USED
C410	C60, 61, 66, 72, 97, 98, 111, 119, 121, 124, 135, 189, 192, 228, 230, 232, 236, 298, 346-400
CR48	CR11-16, 18, 20-31, 38-42, 44
D2	
E10	E1-E8
L28	L3-L5, 13-19, 22
Q79	Q42
K8	
R726	R111, 112, 126, 139, 236, 259, 295, 301, 363, 367, 371, 372, 373, 391, 393-396, 399, 405, 477, 488, 500-508, 511-519, 535, 537, 545, 587, 595, 596, 633, 660, 664, 669, 675, 676, 682-699, 701, 703-708, 710
RP32	RP5, 6, 9, 11, 12, 16, 17, 23, 24
T11	
TP3	
U80	U47
W11	

DO NOT SCALE DRAWING

TOLERANCE

DRAWN J.W. CARROLL — CHECKED — PROJ ENG. — MANUFACTURING — QUALITY ASSUR — ENG. SERV — DATE

DASH NO — NUMBER — QTY — NEXT ASSEMBLY

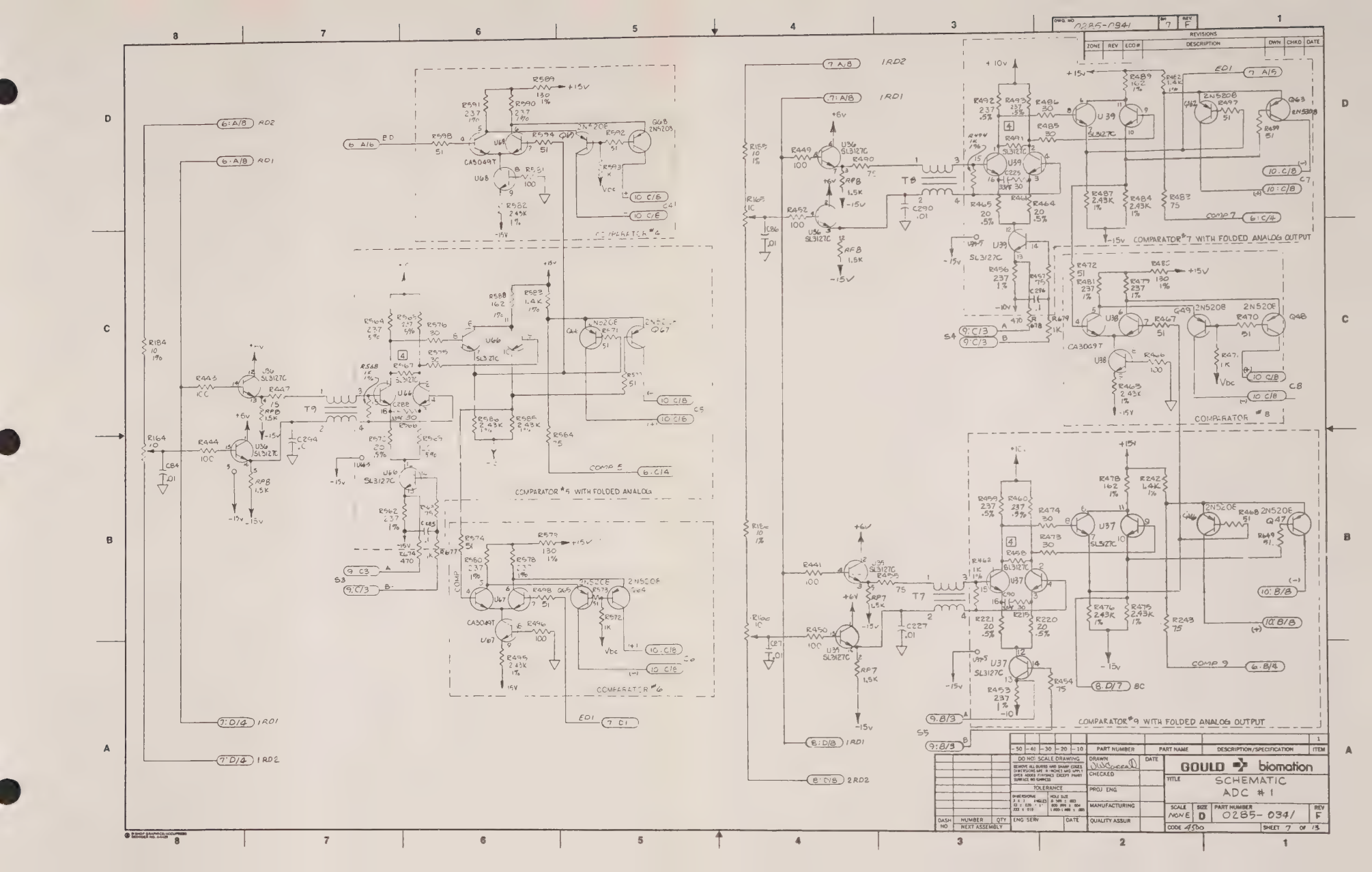
PART NUMBER — PART NAME — DESCRIPTION/SPECIFICATION — ITEM

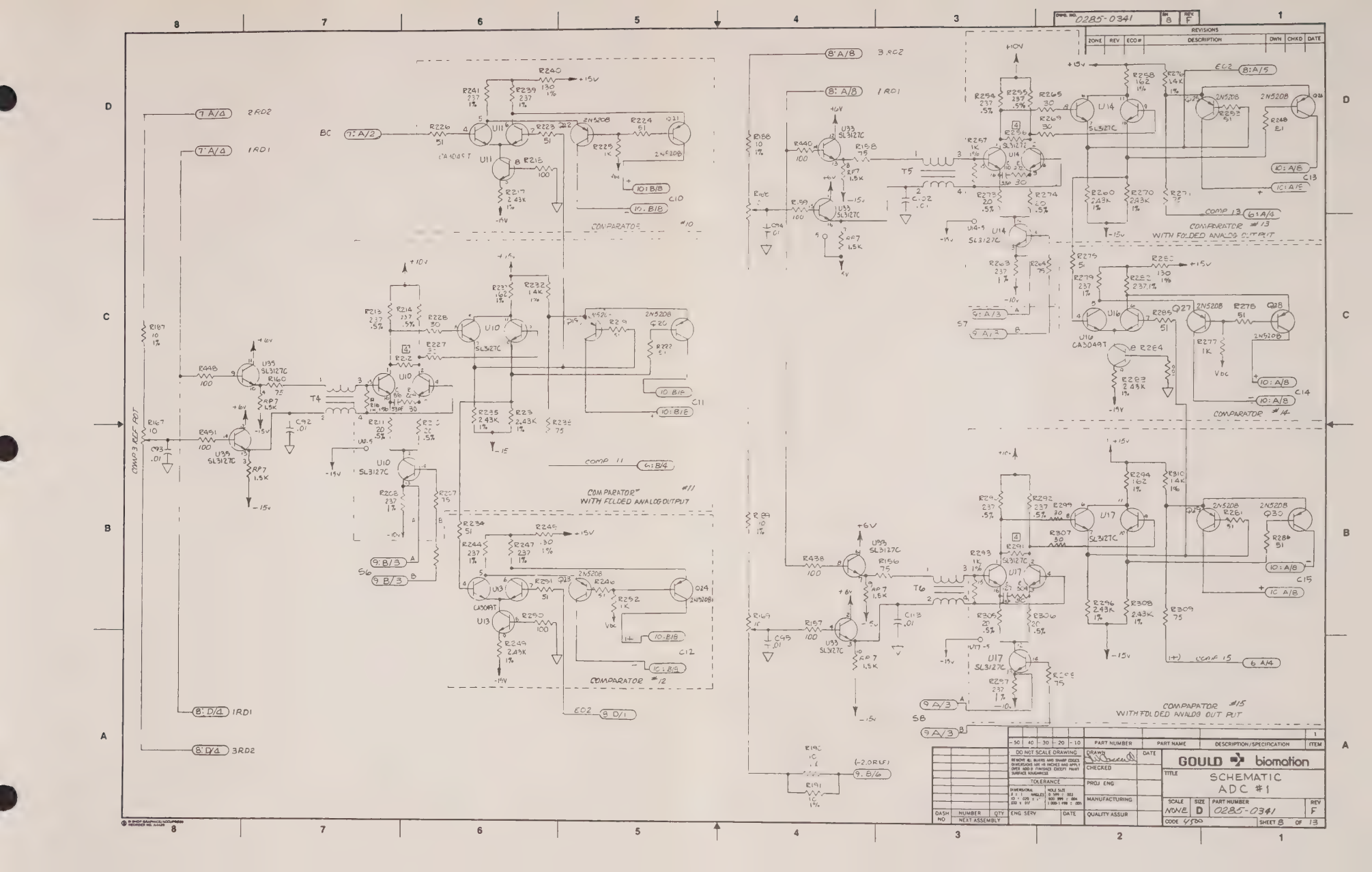
GOULD biomation

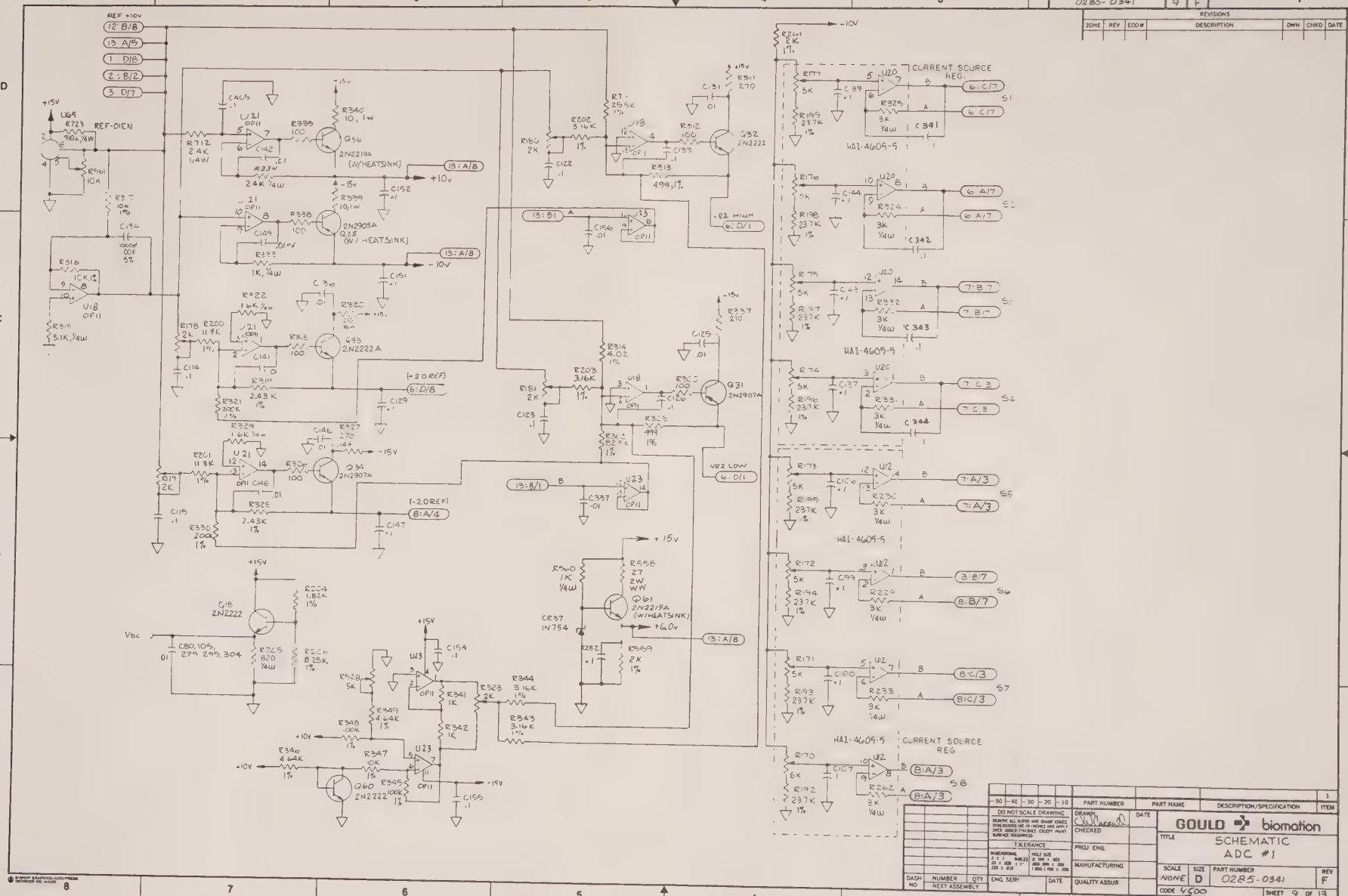
TITLE: SCHEMATIC ADC #1

SCALE ~ — SIZE D — PART NUMBER 0285-0341 — REV F

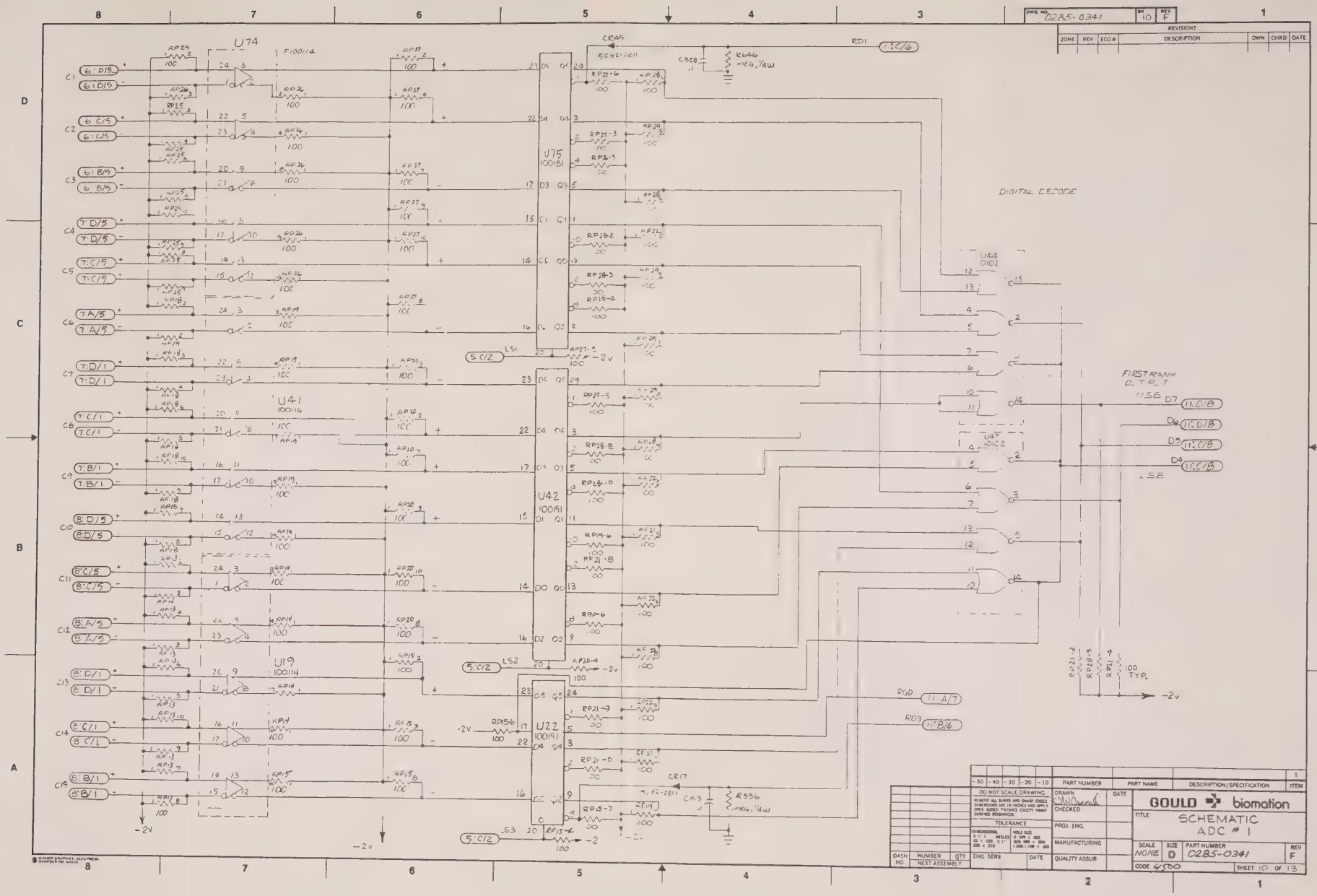
CODE 4500 — SHEET 6 OF 13


COMPARATOR #4
COMPARATOR #5 WITH FOLDED ANALOG
COMPARATOR #6
COMPARATOR #7 WITH FOLDED ANALOG OUTPUT
COMPARATOR #8
COMPARATOR #9 WITH FOLDED ANALOG OUTPUT
DWG NO 0285-0941
REVISIONS
GOULD biomation
SCHEMATIC
ADC #1
PART NUMBER 0285-0341
SHEET 7 OF 13

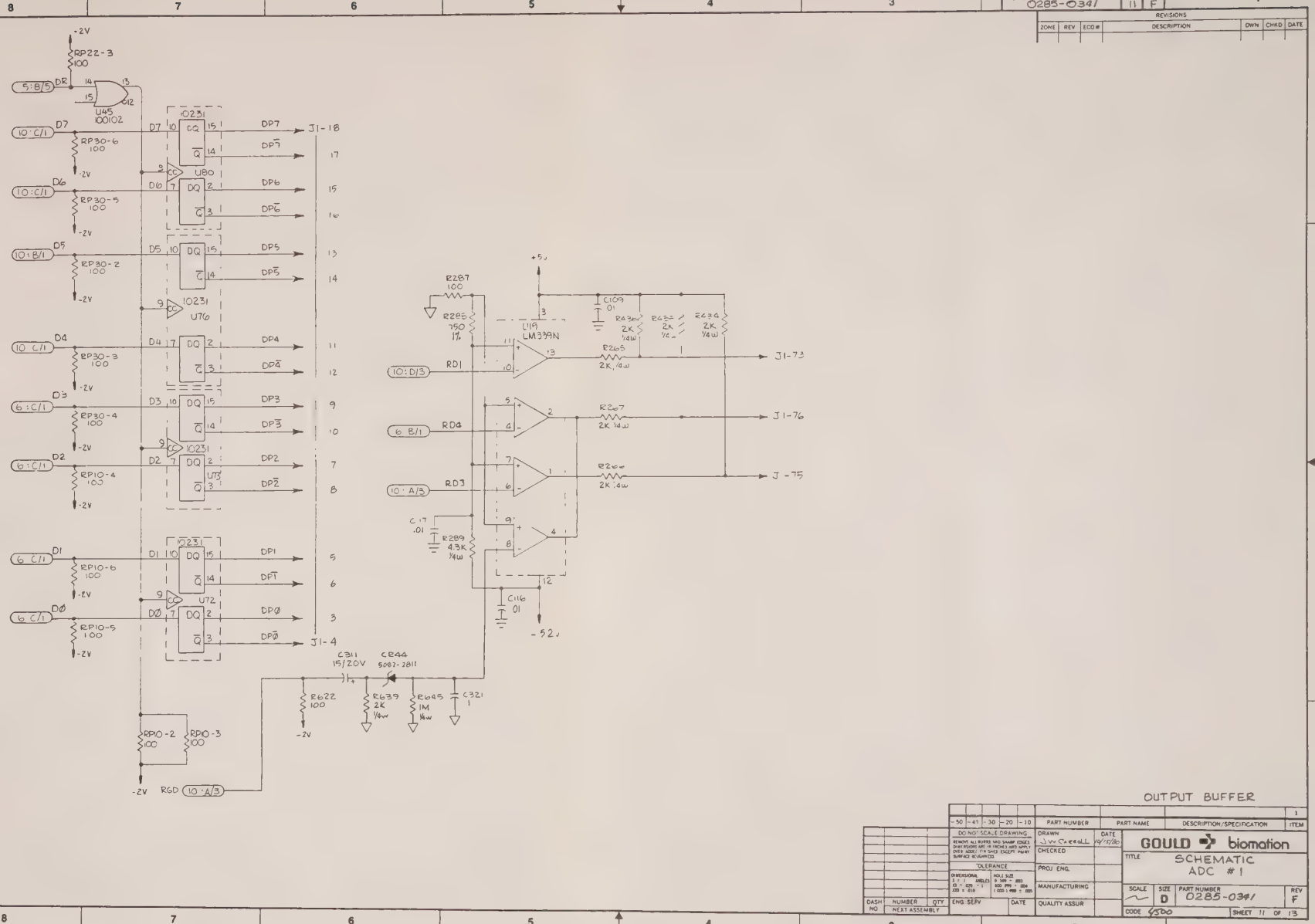

0285-0341
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SCHEMATIC
ADC #1
GOULD biomation
SCALE NONE SIZE D PART NUMBER 0285-0341 REV F
CODE 47580 SHEET 8 OF 13
COMPARATOR #10
COMPARATOR #11
WITH FOLDED ANALOG OUTPUT
COMPARATOR #12
COMPARATOR #13
WITH FOLDED ANALOG OUTPUT
COMPARATOR #14
COMPARATOR #15
WITH FOLDED ANALOG OUT PUT
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DASH NO
NUMBER NEXT ASSEMBLY
QTY



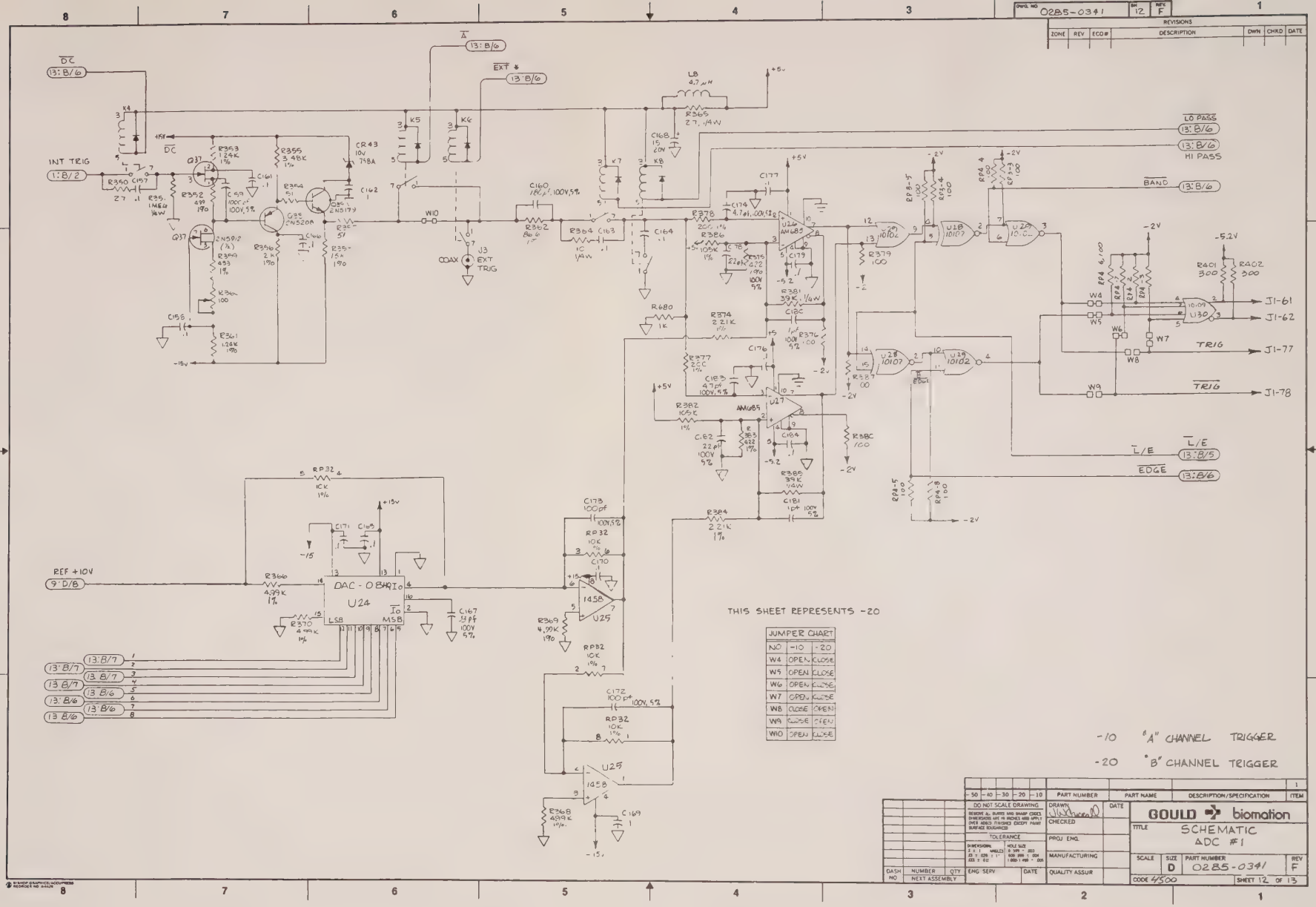
DWG. NO. 0285-0341
SH 9
REV F
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
REF +10V
12 B/8
13 A/5
1 D/8
2 B/2
3 D/7
REF-01EN
CURRENT SOURCE REG.
HA1-4605-5
CURRENT SOURCE REG
Q56 2N2219A (W/HEATSINK)
Q35 2N2905A (W/HEATSINK)
Q33 2N2222A
Q34 2N2907A
Q32 2N2222
Q31 2N2907A
Q61 2N2219A (W/HEATSINK)
Q18 2N2222
Q60 2N2222
VR2 HIGH
VR2 LOW
(+20REF)
(-20REF)
Vbc
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
SCHEMATIC
ADC #1
SCALE NONE
SIZE D
PART NUMBER 0285-0341
REV F
CODE 4500
SHEET 9 OF 13



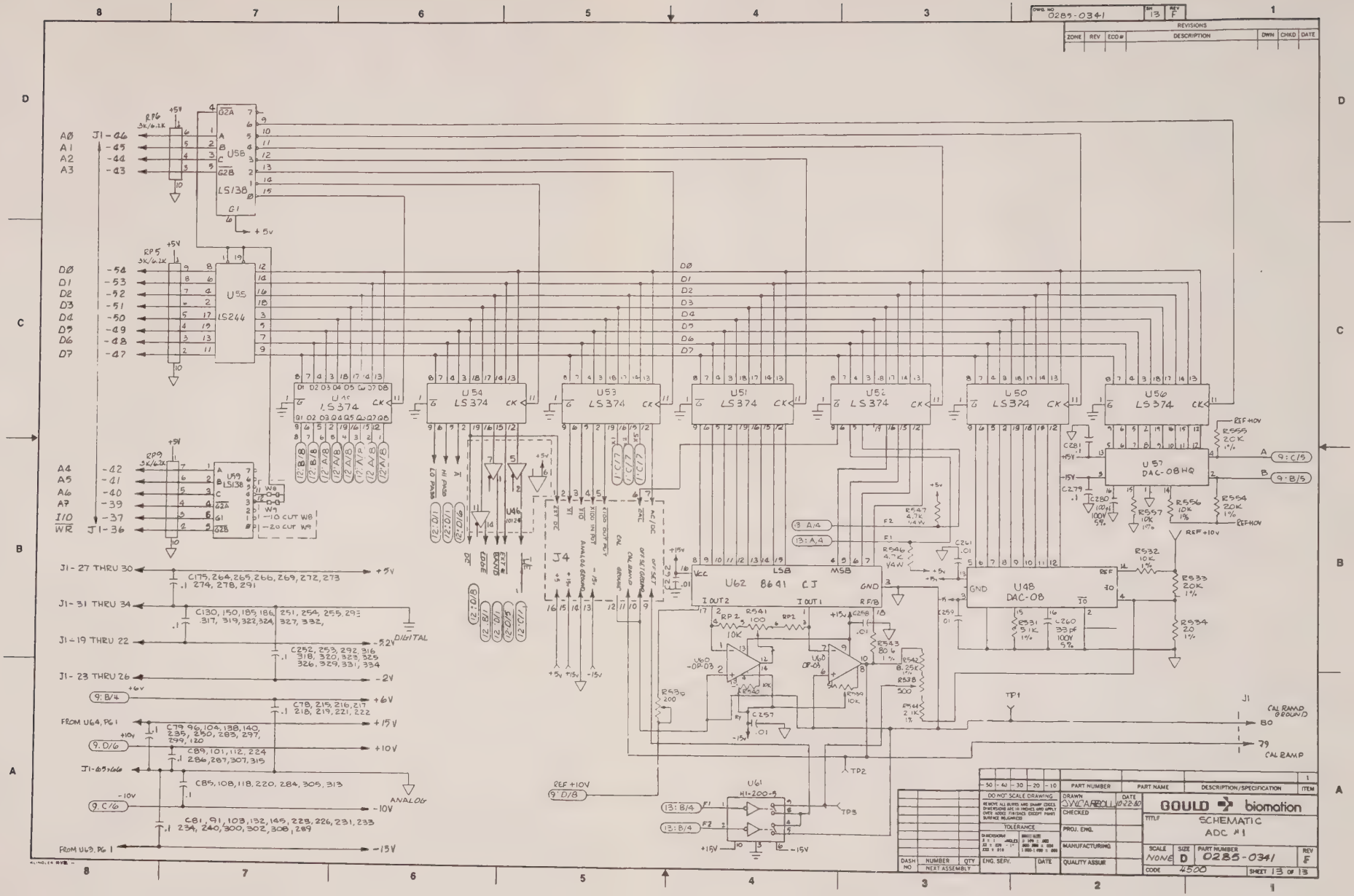
DWG NO 0285-0341
SH 10
REV F
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
U74
F100114
U75
100151
U41
100114
U42
100151
U19
100114
U22
100151
U44
0102
U43
0102
DIGITAL DECODE
FIRST RANK OUTPUT
NSB
LSB
RD1
RD0
RD3
CR45
CR17
R646 MEG, 1/4W
R336 MEG, 1/4W
100 TYP.
-2V
DO NOT SCALE DRAWING
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
SCHEMATIC
ADC # 1
SCALE NONE
SIZE D
PART NUMBER 0285-0341
REV F
CODE 4500
SHEET 10 OF 13



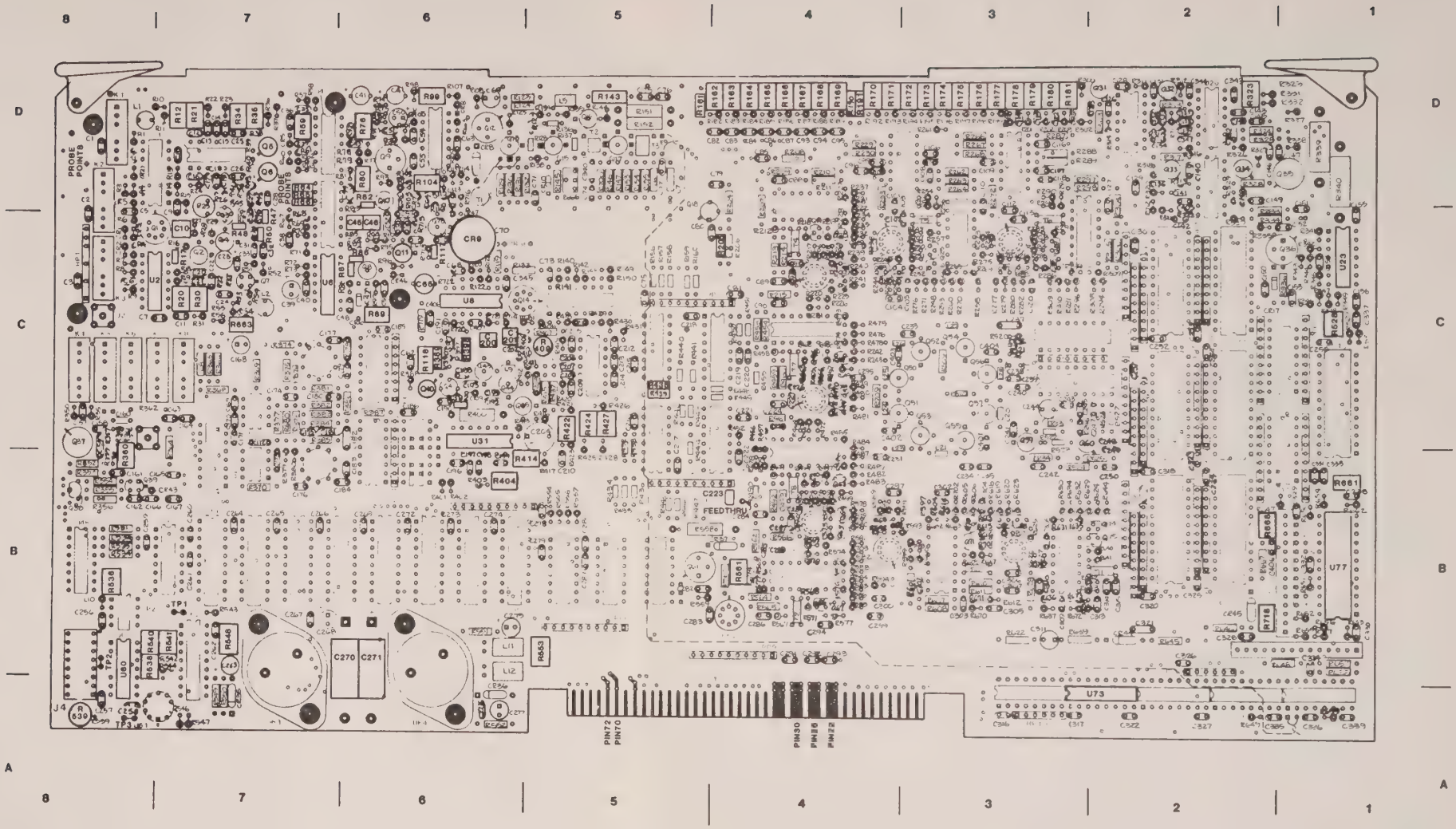
DWG. NO 0285-0341
SH 11
REV F
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
-2V
RP22-3 100
5:B/5
DR
U45 100102
10:C/1
D7
RP30-6 100
10231
U80
DP7
DP7̄
J1-18
D6
RP30-5 100
DP6
DP6̄
10:B/1
D5
RP30-2 100
DP5
DP5̄
U76
D4
RP30-3 100
DP4
DP4̄
6:C/1
D3
RP30-4 100
DP3
DP3̄
U73
D2
RP10-4 100
DP2
DP2̄
D1
RP10-6 100
DP1
DP1̄
U72
DØ
RP10-5 100
DPØ
DPØ̄
J1-4
RP10-2 100
RP10-3 100
RGD
10:A/3
R287 100
R285 750 1%
+5V
U19 LM339N
C109 .01
R436 2K 1/4W
R435 2K 1/4W
R434 2K 1/4W
R265 2K 1/4W
J1-73
10:D/3
RD1
6:B/1
RD4
R267 2K 1/4W
J1-76
10:A/3
RD3
R266 2K 1/4W
J-75
C17 .01
R289 4.3K 1/4W
C116 .01
-52V
C311 15/20V
CR44 5082-2811
R622 100
R639 2K 1/4W
R645 1M 1/4W
C321 1
OUTPUT BUFFER
-50 -45 -30 -20 -10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
DRAWN J.W. Carroll
DATE 10/15/80
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC ADC #1
SCALE
SIZE D
PART NUMBER 0285-0341
REV F
CODE 4500
SHEET 11 OF 13



JUMPER CHART		
NO	-10	-20
W4	OPEN	CLOSE
W5	OPEN	CLOSE
W6	OPEN	CLOSE
W7	OPEN	CLOSE
W8	CLOSE	OPEN
W9	CLOSE	OPEN
W10	OPEN	CLOSE



DWG. NO 0285-0341
SH 13
REV F
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
A0 J1-46
A1 -45
A2 -44
A3 -43
D0 -54
D1 -53
D2 -52
D3 -51
D4 -50
D5 -49
D6 -48
D7 -47
A4 -42
A5 -41
A6 -40
A7 -39
I/O -37
WR J1-36
U58 LS138
U55 LS244
U59 LS138
U54 LS374
U53 LS374
U51 LS374
U52 LS374
U50 LS374
U56 LS374
U57 DAC-08HQ
U48 DAC-08
U62 8641 CJ
U60 OP-03
U61 HI-200-5
J4
J1-27 THRU 30
J1-31 THRU 34
J1-19 THRU 22
J1-23 THRU 26
FROM U64, PG 1
J1-65&66
FROM U63, PG 1
DIGITAL
ANALOG
CAL RAMP GROUND
CAL RAMP
REF +10V
REF +10V
TP1
TP2
TP3
J1
80
79
GOULD biomation
TITLE SCHEMATIC ADC #1
SCALE NONE
SIZE D
PART NUMBER 0285-0341
REV F
CODE 4500
SHEET 13 OF 13
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV.
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM



PROBE POINTS
FEEDTHRU
PIN72
PIN70
PIN30
PIN26
PIN22

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1					1	1	0285-0267	P.C. BOARD				
2					REF	REF	0285-0266	SCHEMATIC				
3					1	1	1100-0026	DIODE	CR7	IN942A		
4					2	2	1100-0006	DIODE	CR43, 47	758A		
5					4	4	1000-0003	DIODE	CR1, 2, 3, 4 17, 32, 44, 45, 46	5082-2811		
6												
7					1	1	1000-0024		CR9	D4858	DIODE BRIDGE	ALPHA
8					3	3	1100-0003		CR6, 8, 10	IN751		
9					2	2	1100-0005		CR19, 34	IN755A		
10					2	2	1100-0015		CR5, 33	IN825		
11					1	1	1100-0016	DIODE	CR37	IN754		
12					3	3	1200-0001	RECTIFIER	CR35, 36, 48	IN4002		
13												
14					8	8	1300-0001	TRANSISTOR	Q5, 6, 18, 32 33, 40, 41, 60	2N2222		
15					2	2	1300-0006	TRANSISTOR	Q1, 36	2N2219A		
16						1	1300-0007	TRANSISTOR	Q39	2N5179		

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROD REL PER ERN # 266	2/5/82	[illegible]	R	5/11/82
B	REVISED PER ECO # 2726	[illegible]	[illegible]	[illegible]	[illegible]
C	REVISED PER ECO # 2729	6/15/82	[illegible]	[illegible]	[illegible]
D	REVISED PER ECO # 2734	8/2/82	[illegible]	[illegible]	[illegible]

DRAWN	DATE
CHECKED R. Dean	6/11/82
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

-1C | 0285-0266 | QTY
DASH NO. | NUMBER | NEXT ASSEMBLY

LIST OF MATERIAL

ASSEMBLY
ADC #1 BOARD

MODEL 450

biomation

B | 0285-0340 | REV D

CODE | SHEET 1 OF 2

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
17												
18					9	9	1300-0058	TRANSISTOR	Q4, 11, 13, 15, 16 44, 45, 76, 77	BFR-96		
19					2	2	1400-0001		Q31, 34	2N2907A		
20					2	2	1400-0003		Q9, 35	2N2905A		
21					1	1	1400-0014		Q12	2N5583		
22					15	15	1400-0029		Q21-24, 27, 28, 48, 49, 64, 65, 68, 69, 72, 73 38	2N5208		
23					5	5	1400-0040		Q2, 8, 43, 59, 78	ON586		
24					2	2	1400-0041		Q17, 78	BFT-96		
25					3	3	1500-0006		Q1, 14, 37	2N5912		
26					3	3	1500-0019	TRANSISTOR	Q3, 7, 10	MFE52		
27					1	1	9000-0132	TRANSISTOR	Q50-57		MATCHED SET 8 PIECES	
28					1	1	9000-0133	TRANSISTOR	Q19, 20, 25, 26 29, 62, 63, 66, 67, 70, 30, 46, 47, 71, 74, 75		MATCHED SET 8 PIECES	
29												
30												
31												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO | NUMBER | QTY
NEXT ASSEMBLY

LIST OF MATERIAL

ASSEMBLY
ADC #1 BOARD

MODEL 450

biomation

B | 0285-0340 | REV D

CODE | SHEET 2 OF 2

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
32					7	7	1700-0008	I.C.	U11,13,16,38 67,68,70	CA3049T		
33					.	1	1700-0018		U25	1458		
34					15	15	1700-0032-20		U1,5,9,10,14,17,33 34,35,36,37,39	SL3127C	MFG. PLESSY	
									66,69,71			
35						1	1700-0038		U15	LM339N		
36					1	1	1700-0063-20		U65	REF-01EJ	MFG. PMI	
37					1	1	1700-0089		U63	LM337K		
38					1	1	1700-0090		U64	LM317K		
39					1	1	1700-0098		U60	OP-03		
40					7	7	1700-0099		U3,4,7,12,20,31,32	HA4605		
41					3	3	1700-0100		U2,6,8	SL2364C		
42					1	1	1700-0105		U61	HI-200-5		
43					3	3	1700-0106		U18,21,23	OP11EP		
44					2	2	1800-0193		U58,59	74LS138		
45					1	1	1800-0240		U55	74LS244		
46					7	7	1800-0293		U49,50,51,52 53,54,56	745374		
47					1	1	1820-0075		U62	8641		
48					3	3	1850-0002	I.C.	U29,43,44	10102		

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSEMBLY

ADC #1 BOARD

biomation

B | 0285-0340 | REV D

MODEL 4500 | CODE | SHEET 3 OF 18

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
49					1	1	1850-0021	I.C.	U46	10124		
50					1	1	1850-0022		U28	10107		
51					1	1	1850-0026		U30	10109		
52					1	1	1850-0047		U78	11C70		
53					1	1	1850-0049		U79	MC10103		
54					2	2	1850-0071		U26,27	AM685		
55					1	1	1850-0078		U45	100102		
56					4	4	1850-0080		U19,41,74,77	100114		
57					3	3	1850-0085		U22,42,75	100151		
58					1	1	1850-0092		U40	AM6688		
59					4	4	1850-0097		U72,73,76,80	MC10231L		
60					2	2	1900-0012		U24,57	DAC08HQ		
61					1	1	1900-0007	I.C.	U48	DAC-08		
62												
63												
64												
65					1	1	2950-2707	RESISTOR	R350		2.7Ω, 1/8W, 5%	
66					4	4	2950-.006	RESISTOR	R 34 135, 36, 522		0Ω 1/8W, 5%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSEMBLY

ADC #1 BOARD

biomation

B | 0285-0340 | REV D

MODEL 4500 | CODE | SHEET 4 OF 18

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
67												
68					27	27	2950-3006	RESISTOR	R70,83,209,215,227, 228,265,269,272 299,304,307,461 473,474,485,486,523, 566,575,576,601,602 603 628,631,635		30Ω, 1/8W, 5%	
69					1	1	2950-3306		R650		33Ω	
70					48	48	2950-5106		R119,154,155,219,223,224 226,234,246,251,253,275, 278,281,285,354,357,467, 468,470,472,497,498,571, 573,574,592,594,598,615, 621,625,640,647,652, 653,654,613,6,614,694,577 499,469,222,248,286,721		51Ω	
71					25	25	2950-7506		R125,156,158,160,238,243, 271,309,445,446,447,455 490,584,605,629,483,207, 264,298,454,457,563, 607,636		75Ω	
72					70	70	2950-1000	RESISTOR	R4,7,13,17,19,27,38,40,69 72,81,86,96,109,121,128 137,141,142,144,157,159,287, 300,312,318,326,335,338 376,379,380,387,388 390,398, 413,430,432,433,438,439 440,441,442,443,449,448, 449,450,451,452, 510,526,527,529,530,581 622,651,657,658,659 662,663,699,713,714,716,722		100Ω, 1/8W, 5%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
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	QUALITY ASSURANCE	

LIST OF MATERIAL

ASSEMBLY

ADC #1 BOARD

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COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
73					3	3	2950-2000	RESISTOR	R45,53,93		200Ω, 1/8W, 5%	
74												
75					2	2	2950-2700		R311,337		270Ω	
76					2	2	2950-3000		R401,402		300Ω	
77					16	16	2950-1001		R74,225,252,277,341,342,678, 593,572,471,671,673,677,679,680,85		1K, 1/8W, 5%	
78					5	5	2950-4700		R672,670,674,678,681		470, 1/8W, 5%	
79					2	2	2950-1100		R655,656		110Ω, 1/8W, 5%	
80												
81												
82					1	1	3000-3006		R437		30Ω, 1/4W, 5%	
83					1	1	3000-1006		R364		10Ω, 1/4W, 5%	
84					1	1	3000-7506		R416		75Ω	
85					4	4	3000-1000		R52,92,2,87		100Ω	
86					2	2	3000-1200		R550,551		120Ω	
87					1	1	3000-1300		R415		130Ω	
88					1	1	3000-1500		R145		150Ω	
89					1	1	3000-1600	RESISTOR	R51		160Ω, 1/4W 5%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
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LIST OF MATERIAL

ASSEMBLY

ADC #1 BOARD

biomation

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COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
90					1	1	3000-2200	RESISTOR	R49		220Ω, 1/4W, 5%	
91					2	2	3000-2700		R320, 327		270Ω	
92					2	2	3000-6200		R133, 648		620Ω	
93					1	1	3000-6800		R107		680Ω	
94					1	1	3000-8200		R205		820Ω	
95					2	2	3000-9100		R43, 50		910Ω	
96					15	15	3000-1001		R42, 55, 333, 549, 552, 569, 616, 58, 695, 666, 218, 250, 284, 700, 715		1K	
97					1	1	3000-4300		R105		430Ω	
98					2	2	3000-1601		R322, 329		1.6K	
99					2	2	3000-1801		R39, 719		1.8K	
100					15	15	3000-2001		R266, 267, 268, 434, 435, 436, 52, 689, 701, 702, 704, 705, 706, 707, 708		2K	
101					2	2	3000-2201		R101, 525		2.2K	
102					7	7	3000-2701		R24, 32, 46, 102, 365, 431, 524		2.7K	
103					4	4	3000-3601		R58, 78, 90, 420		3.6K	
104												
105					3	3	3000-4301		R41, 289, 509		4.3K	
106					2	2	3000-4701		R546, 547		4.7K	
107					1	1	3000-5101	RESISTOR	R315		5.1K, 1/4W, 5%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
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LIST OF MATERIAL
ASSEMBLY
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COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
108					1	1	3000-5601	RESISTOR	R61		5.6K, 1/4W, 5%	
109					1	1	3000-6801		R419		6.8K	
110					3	3	3000-1002		R33, 44, 103		10K	
111					2	2	3000-3902		R381, 385		39K	
112					5	5	3000-1004		R336, 351, 520, 645, 646		1M, 1/4W, 5%	
113					1	1	3000-1003		R665		100K, 1/4W, 5%	
114												
115					2	2	3000-2401		R334, 720		2.4K, 1/4W, 5%	
116					8	8	3000-3001		R325, 324, 332, 331, 230, 229, 233, 262		3K, 1/4W, 5%	
117												
118					4	4	3050-1000		R113, 114, 115, 116		100Ω, 1/2W, 5%	
119					2	2	3050-1500		R151, 152		150Ω, 1/2W, 1%	
120					2	2	3070-1006		R339, 340		10Ω, 1W, 5%	
121												
122												
123												
124					11	11	3100-1006		R161, 82, 183, 184, 185, 186, 187, 188, 189, 190, 191		10Ω, 1/8W, 1%	
125					4	4	3100-2616	RESISTOR	R106, 117, 146, 147		26.1Ω, 1/8W, 1%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
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COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
126							3100-4646	RESISTOR	R412		46.4Ω, 1/8W, 1%	
127					1	1	3100-7506		R88		75Ω	
128					1	1	3100-8666		R362		86.6Ω	
129					4	4	3100-1210		R129, 30, 31, 32		121Ω	
130					7	7	3100-1300		R240, 245, 280, 480, 579, 589, 619		130Ω	
131												
132					4	4	3100-2000		R71, 84, 377, 378		200Ω	
133					1	1	3100-2260		R91		226Ω	
134					22	22	3100-2370		R208, 239, 241, 244, 247 263, 279, 282, 297, 453 456, 479, 481, 623, 562 578, 580, 637, 590, 608 591, 620		237Ω	
135					1	1	3100-2610		R15		261Ω	
136					2	2	3100-2740		R47, 389		274Ω	
137					2	2	3100-4220		R375, 383		422Ω	
138					1	1	3100-4530		R359		453Ω	
139												
140					3	3	3100-4990	RESISTOR	R303, 313 352		499Ω .1/8W 1%	

REF DRAWINGS	REV.	DESCRIPTION	DATE	DWN	CKD	APPD

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COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
141					8	8	3100-5110	RESISTOR	R8, 48 54, 73, 120, 122, 407 408		511Ω, 1/8W, 1%	
142					1	1	3100-5066		R543		81Ω	
143					2	2	3100-6810		R429, 411		681Ω	
144					4	4	3100-7500		R67, 153, 288, 410		750Ω	
145					3	3	3100-8250		R3, 56, 9		825Ω	
146					23	23	3100-1001		R2, 5, 14, 26, 29, 66, 68, 87, 94 123, 149, 150, 216, 257, 293, 641, 406, 418, 462, 568, 609 494, 148		1K	
147					2	2	3100-1241		R353, 361		1.24K	
148					3	3	3100-1501		R18, 358, 397		1.5K	
149					1	1	3100-1781		R95		1.78K	
150					3	3	3100-1821		R1, 140, 204		1.82K	
51					5	5	3100-2001		R65, 261, 356, 392, 559		2K	
152					2	2	3100-2211		R374, 384		2.21K	
153					1	1	3100-2321		R60		2.32K	
154					20	20	3100-2431	RESISTOR	R127, 138, 231, 235, 260, 270 296, 308, 314, 328, 475, 476 484, 487, 585, 586, 597 604, 630, 632		2.43K, 1/8W, 1%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

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COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
155					1	1	3100-2611	RESISTOR	R124		2.61K, 1/8W, 1%	
156					7	7	3100-2871		R217, 249, 283, 463, 495, 582, 617		2.87K	
157					5	5	3100-3161		R97, 203 343, 344, 202		3.16K	
158					1	1	3100-3401		R417		3.4K	
159					1	1	3100-3481		R355		3.48K	
160					4	4	3100-4641		R10, 37, 346, 349		4.64K	
161					4	4	3100-4991		R366, 368, 369, 370		4.99K	
162					1	1	3100-5101		R531		5.1K	
163					7	7	3100-5111		R16, 22, 23, 29, 82, 421, 423		5.11K	
164					5	5	3100-8251		R31, 36, 206, 426, 542		8.25K	
165					1	1	3100-9761		R75		9.76K	
166					16	16	3100-1002		R11 57, 63, 79, 98, 100, 108, 110 316, 317, 387, 403, 428, 532 556, 557		10K	
167					2	2	3100-1182		R200, 201		11.8K	
168					2	2	3100-1212		R64, 77		12.1K	
169					2	2	3100-1402		R62, 425		14K	
170					4	4	3100-2002	RESISTOR	R533, 554, 555, 261		20K, 1/8W, 1%	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

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ASSEMBLY
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COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
171					2	2	3100-1003	RESISTOR	R345, 348		100K, 1/8W, 1%	
172					2	2	3100-1053		R382, 386		105K, 1/8W, 1%	
173					2	2	3100-2003		R321, 330		200K, 1/8W, 1%	
174					1	1	3100-8252		R302		82.5K, 1/8W, 1%	
175					8	8	FACTORY SELECT		R212, 256, 291, 458 491, 567, 62, 638		FACTORY SELECT	
176					1	1	3000-2401		R712		2.4K, 1/4W, 5%	
177												
178					8	8	3100-2372		R192-199		23.7K, 1/8W 1%	
179					16	16	3120-2006		R210, 211, 220, 221, 273, 274 305, 306, 464, 465, 569, 570 599, 600, 626, 627		20Ω, 1/8W, .5%	
180					1	1	3100-2101		R544		2.10K, 1/8W 1%	
181					16	16	3120-2370		R213, 214, 254, 255, 290, 292 459, 460, 492, 493, 564, 565 610, 611, 643, 642		237Ω, 1/8W, .5%	
182												
183					1	1	3150-1300		R400		130Ω, 1/4W, 1%	
184					1	1	3150-3326		R143		33.2Ω 1/4W 1%	
85					1	1	3200-0041	RESISTOR	R558		27Ω 2W, WW	
186					1	1	3100-2552	RESISTOR	R711		25.5K 1/8W 1%	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

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DASH NO | NUMBER / NEXT ASSEMBLY | QTY

LIST OF MATERIAL

ASSEMBLY
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COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
187					1	1	3300-0031	POT	R539		10K, RD, TOP ADJ	
188					2	2	3300-0061		R25, 409		2K, RD TOP ADJ	
189					5	5	3300-0077		R661, 663, 660, 668, 536		200Ω, SQ. TOP ADJ	
190					8	8	3300-0103		R162, 163, 164, 165, 166, 167, 168, 169		10Ω, SQ. SIDE ADJ	
191					8	8	3300-0105-10		R170, 171, 172, 173, 174, 175 176, 177		5K, SQ. SIDE ADJ	
192					7	7	3300-0108-10		R21, 34, 404, 414 422, 424, 528		5K, SQ. TOP ADJ	
193					2	2	3300-0109-10		R20, 89		2K, SQ. TOP ADJ	
194					8	8	3300-0110-10		R30, 35, 76 80, 118, 548, 553, 718		1K, SQ. TOP ADJ	
195					8	8	3300-0112-10		R12, 59, 99, 104 427, 540, 561, 666		10K, SQ. TOP ADJ	
196					2	2	3300-0092	POT	R360, 541		100Ω, SQ. TOP ADJ	
197					1	1	3300-0076	POT	R538		500Ω TOP ADJ	
198					5	5	3300-0115	POT	R178, 179, 180 181, 323		2K SIDE ADJ	
199					1	1	3100-4021	RES	R314		4.02K, 1/8W, 1%	
200					1	1	9000-0060	RES PACK	RP1		5 PIN SIP	
201					2	2	3700-0098		RP10, 30		100Ω 6 PIN SIP	
202					3	3	3700-0096		RP3, 4, 31		100Ω, .2W, 2% 8 PIN SIP	
203					13	13	3700-0080	RES PACK	RP13, 14, 15, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29		100Ω 10 PIN SIP	
204												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

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	NEXT ASSEMBLY	

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COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
205					2	2	3700-0062	RES PACK	RP7, 8		1.5K 10 PIN SIP	
206					3	3	3700-0049	RES PACK	RP5, 6, 9		3K/6.2K 10 PIN SIP	
207					2	2	3700-0079	RES PACK	RP2, 32		10K 8 PIN DIP	
208												
209												
210												
211					64	64	4000-0044	CAPACITOR	C1, 2, 3, 4, 6, 8, 11, 20, 28, 29, 40, 44, 47, 62, 68, 74, 80, 82 83, 84, 86, 87, 92, 93, 94, 95 102, 105, 109, 113, 116, 117, 125, 131, 136, 141, 146, 156, 188, 195, 211, 227, 229 241, 242, 243, 245, 246, 247 257, 258, 259, 261, 262, 290 294, 295, 149, 304, 306, 142, 314, 337, 148		.01μf, 100V, 20%	
212					188	183	4010-0104	CAPACITOR	C13, 14, 15, 17, 18, 19, 24, 27, 32, 33, 34, 35, 36, 37, 39, 42, 43, 48, 51, 53, 54, 58, 59 63, 64, 73, 75, 76, 77, 78, 79, 81, 85, 89, 91, 96, 99, 100, 101, 103, 104, 106, 107, 108, 112, 114, 15, 118, 120, 122, 123, 129, 130 32, 137, 138, 139, 140, 143, 144, 145, 147, 150, 151, 152, 153, 154, 155, 157, 158, 161 ~ 165, 166, 169 170, 171, 175, 176, 177, 179, 184, 185, 186, 187, 190, 193		.1μf, 50V, 20% CONT. SHT	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
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COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
								CAPACITOR	C196, 197, 198, 206, 207, 208, 210, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 234 226, 231, 233 235, 240. 248, 249, 250, 251, 252, 253, 254, 256, 264, 265, 266, 267, 269, 272, 274, 276, 278, 279 281, 282, 283, 284, 286, 287, 289, 291, 292, 293, 297, 299 300, 302, 305, 307, 308, 313 315, 316, 317, 318, 319, 320, 322, 323, 324, 325, 326, 327, 328, 329, 331, 332, 406, 334, 336, 339, 273, 255, 285, 296, 303, 309, 401-408, 126, 133, 34- 344, 406		.1uf, 50V, 20%	
213					3	3	4300-0026		C238, 311, 244		15uf, 20V	
214					5	5	4000-0007		C52, 57, 203 237, 321		1uf, 50V, 20%	
215												
216					9	9	4300-0015		C23, 39, 50, 69, 263, 268, 275, 277, 168		15uf, 20V	
217					2	2	4300-0008		C270, 271		47uf, 20V	
218					1	1	4300-0028		C204		100uf, 20V	
219					1	1	4300-0045		C65		220uf, 10V	
220					2	2	4300-0024		C49, 41		4.7uf, 50V, 10%	
221					1	1	4010-8206		C338		8.2 pf 100V, 5%	
222					3	3	4010-1006	CAPACITOR	C67, 180, 18		1pf, 100V, 5%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

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COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
223					2	2	4010-2206	CAPACITOR	C21, 202		2.2 pf, 100V, 5%	
224					4	4	4010-4706		C9, 174, 183, 330		4.7 pf, 100V, 5%	
225					1	1	4010-6806		C70		6.8 pf, 100V, 5%	
226					3	3	4010-0100		C239, 333, 407		10 pf, 100V. 5%	
227												
228					2	2	4010-0220		C178, 182		22pf, 100V, 5%	
229					10	10	4010-0330		C88, 90, 110, 127, 167, 225, 260, 286, 301, 310		33 pf, 100V, 5%	
230					2	2	4010-0470		C31, 71		47pf, 100V, 5%	
231												
232					7	7	4010-0101		C7, 172, 173, 191, 205, 212, 280		100pf, 100V, 5%	
233					2	2	4010-0181		C160, 340		180pf, 100V, 5%	
234					1	1	4010-0221		C199		220pf, 100V, 5%	
235					12	12	4010-0102		C5, 16, 22, 26, 30, 55, 56, 134, 189, 196, 209, 345		1000pf, 100V, 5%	
236												
237												
238					5	5	4600-0016	VAR. CAPACITOR	C10, 45, 46, 200, 201		1 - 4.5 pf	
239					2	2	4010-0102	CAP	C12, 25		1000pf, 100V, 5%	
240												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO | NUMBER | QTY | NEXT ASSEMBLY

LIST OF MATERIAL

ASSEMBLY
ADC #1 BOARD

biomation

B | 0285-0340 | REV D

MODEL 4500 | CODE | SHEET 16 OF 18

COMMENTS		TOTAL COST	UNIT COST
[1] -10 ONLY			

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
241					2	2	2100-0005	INDUCTOR	L6,7		1uh	
242					1	1	2100-0002		L8		4.7uh	
243					1	1	2100-0007		L10		10 uh	
244					1	1	2100-0001		L9		FERRITE BEAD	
245					4	4	9000-0091		L1,2,11,12		2½ TURNS #22 WIRE ON 6 HOLE SHIELD BEAD	
246					1	1	9000-0088	INDUCTOR	L5		8 TURNS #22 WIRE ON TOROID CORE	
247					8	8	2100-0036-20	INDUCTOR	L20,21,23,24,25,26	27,28	FERRITE BEAD	
248												
249					8	8	9000-0089	TOROID	T4,5,6,7,8,9,10 11		4 TURNS	
250					1	1	9000-0090-10	TOROID	T3		8 TURNS	4M
251					1	1	9000-0090-20	TOROID	T1			1M
252					1	1	9000-0115	TOROID	T2			1M
253												
254												
255					2	2	2150-0007	DELAY LINE	D1,2	EP6700-1	10NS	
256					1	1	0285-0248	SHIELD				
257												
258					6	8	2600-0013	RELAY	K1,2,3,4,7,8 [1].516		741A-10	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO. | NUMBER | QTY | NEXT ASSEMBLY

LIST OF MATERIAL

ASSEMBLY
ADC #1 BOARD

biomation

B | 0285-0340 | REV D

MODEL 4500 | CODE | SHEET 17 OF 18

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
259					7	7	7000-0381		TO BE USED AT U11,13,16,38,66	LOCATION 68,70	MOUNTING PAD	
260					2	2	6000-0134	CONN. COAX	J2,3			
261					1	1	6100-0120	SOCKET	J4		16 PIN	
262					2	2	7000-0120	EJECTOR				
263					3	3	7000-0041	HEAT SINK	Q35,36,61		TO-5, .75 DIA	
264					1	1	7000-0125	HEAT SINK	TO BE USED AT LOCATION U40			
265					2	2	7200-0016	INSULATOR	U63.64			
266												
267					A/R	A/R	9000-0117	TRIFILAR WIRE	E9		.5 LG MIN	
268												
269					3	3	0285-0311	TEST POINTS	TP1,2,3			
270					1	1	3000-3000	RESISTOR	R717		300Ω, 1/4W, 5%	
271					1	1		CAP	C41		4.7uf, 50V	
272					8	8	3100-1620	RESISTOR	R634,702,588,489, 478,237,258,294		162Ω, 1/8W, 1%	
273					8	8	3100-1401	RESISTOR	R232,242,276,310, 482,582,[illegible],624		1.4K, 1/8W, 1%	
274					1	1	3100-2400	RESISTOR	R709		240Ω, 1/4W, 5%	
275					1	1	3100-2006	RESISTOR	R534		20Ω 1/8W 1%	
276												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO | NUMBER | QTY | NEXT ASSEMBLY

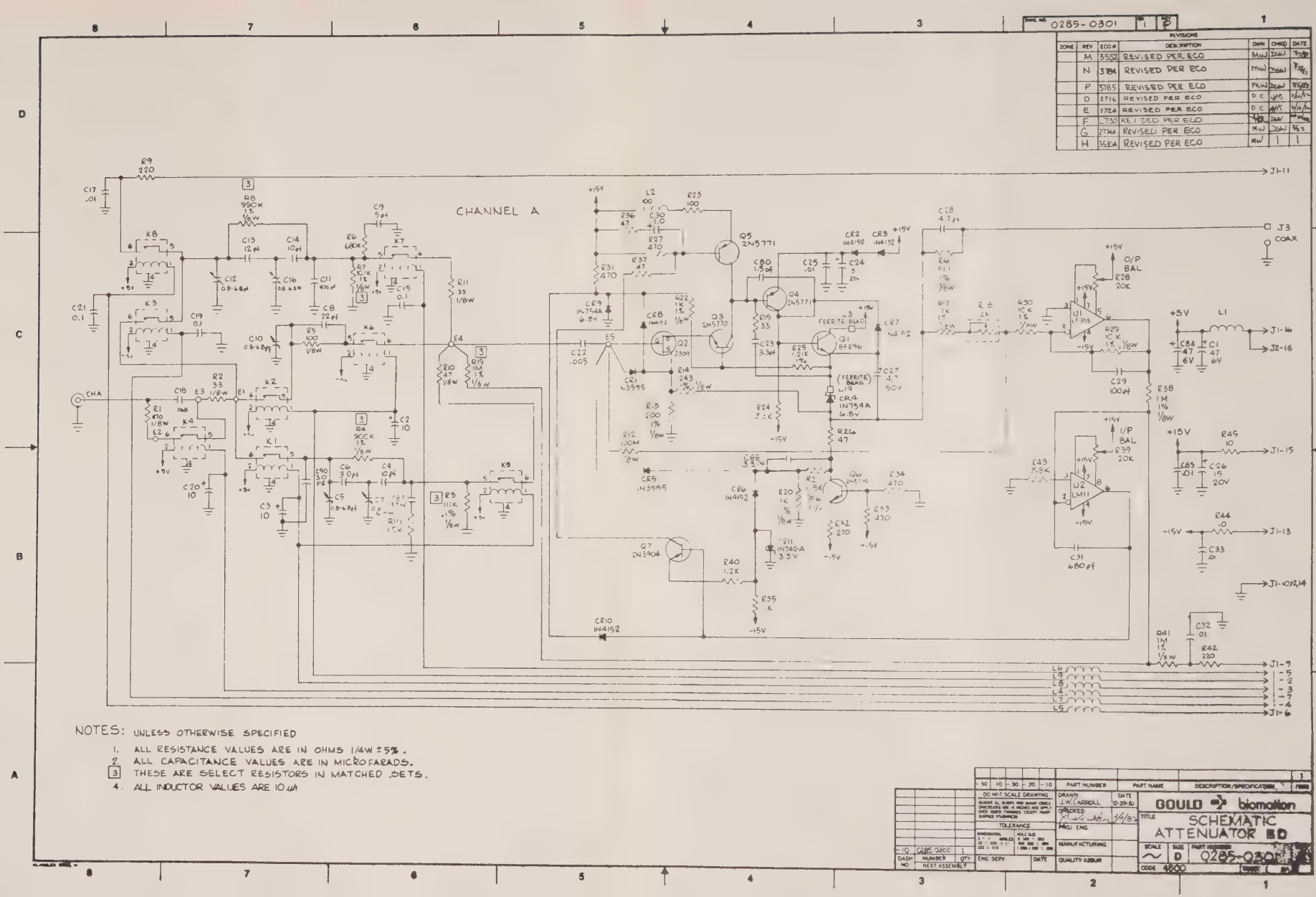
LIST OF MATERIAL

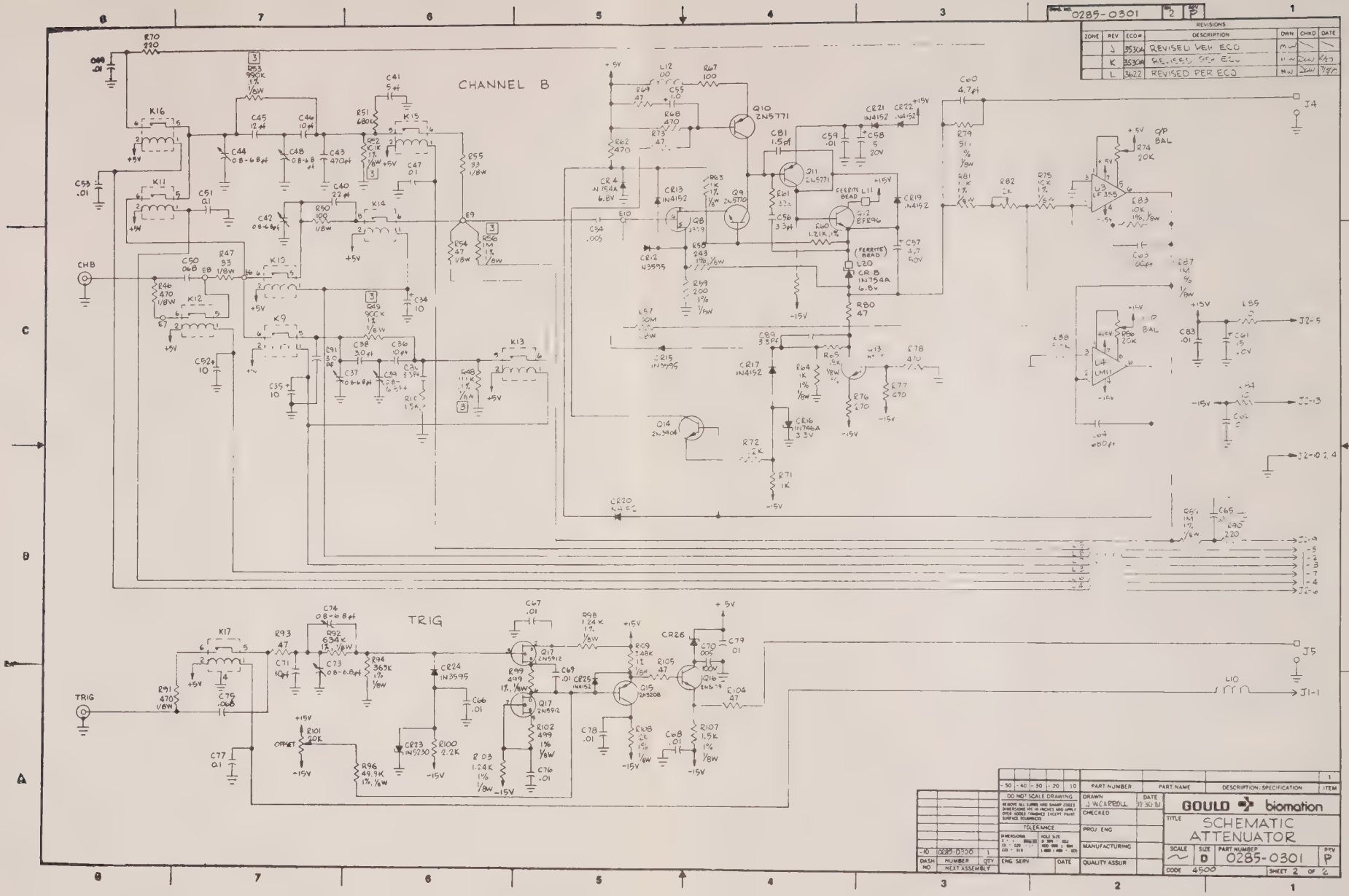
ASSEMBLY
ADC #1 BOARD

biomation

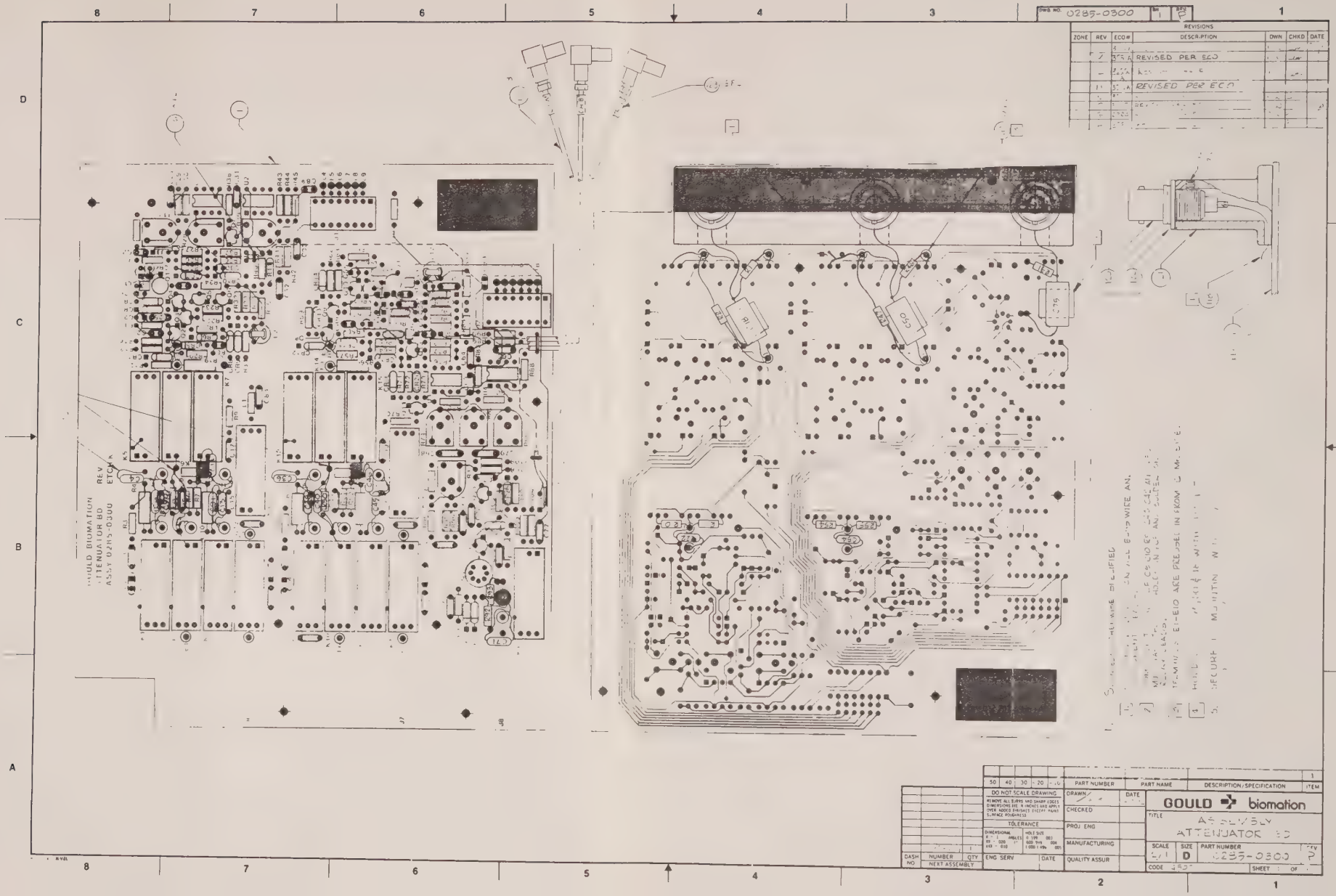
B | 0285-0340 | REV D

MODEL 45[illegible] | CODE | SHEET [illegible] OF [illegible]


0285-0301
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
M 3552 REVISED PER ECO
N 3784 REVISED PER ECO
P 5185 REVISED PER ECO
D 2716 REVISED PER ECO
E 2726 REVISED PER ECO
F 2730 REVISED PER ECO
G 2734 REVISED PER ECO
H 3534 REVISED PER ECO
CHANNEL A
J1-11
J3 COAX
J1-16
J2-16
J1-15
J1-13
J1-10,12,14
J1-9
J1-5
J1-2
J1-3
J1-7
J1-4
J1-6
CHA
O/P BAL
I/P BAL
U1 LF355
U2 LM11
Q1 BF496
Q2 J309
Q3 2N5770
Q4 2N5771
Q5 2N5771
Q6 2N5110
Q7 2N3904
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES ARE IN OHMS 1/4W ±5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3 THESE ARE SELECT RESISTORS IN MATCHED SETS.
4. ALL INDUCTOR VALUES ARE 10 uh
DO NOT SCALE DRAWING
TOLERANCE
DRAWN J.W. CARROLL 12-29-81
CHECKED 2/4/82
MFG. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
GOULD biomation
TITLE SCHEMATIC ATTENUATOR BD
SCALE ~ SIZE D PART NUMBER 0285-0301
CODE 4500



0285-0301
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
J 3530A REVISED PER ECO
K 3530A REVISED PER ECO
L 3622 REVISED PER ECO
CHANNEL B
TRIG
CHB
TRIG
J4
J5
J2-5
J2-13
J2-10 2,4
J1-1
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN J.W.CARROLL
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC ATTENUATOR
SCALE
SIZE D
PART NUMBER 0285-0301
REV P
CODE 4500
SHEET 2 OF 2
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE



DWG NO. 0285-0300
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
REVISED PER ECO
REVISED PER ECO
GOULD BIOMATION
ATTENUATOR BD
ASSY 0285-0300
REV
ETCH K
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY
OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL
HOLE SIZE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
DATE
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
ASSEMBLY
ATTENUATOR BD
SCALE
SIZE
D
PART NUMBER
0285-0300
REV
P
CODE
SHEET
OF

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0285-0302	P.C.B.				
2						REF	0285-0301	SCHEMATIC				
3												
4												
5												
6												
7						2	1700-0108	I.C.	U2,4		LM11CLN	
8						2	1700-0104	I.C.	U1,3		LF355	
9												
10						13	1000-0002	DIODE	CR2,3,6,7,8,10, 13,17,19,20,21,22,	25	IN4152	
11						5	1000-0018	"	CR1,5,12,15,24		IN3595	
12						2	1100-0001		CR11,16		IN746A 3.3V	
13						4	1100-0016	"	CR9,14,18,4		IN754A, 6.8V	
14						1	1100-0044	DIODE	CR23		IN5230	
15						1	1100-0006	DIODE	CR26		IN758A, 10V	
16												
17						4	1300-0046	TRANSISTOR	Q3,6,9,13		2N5770	
18						4	1400-0036	TRANSISTOR	Q4,5,10,11		2N5771	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
G	REVISED PER ECO 2724	8/8/82	D.C.		
B	REVISED PER ECO 2435	3/29/82	TMB		
C	REVISED PER ECO No 2660	5/[illegible]/82	JWC	T.J.	
C	Prod. Rel. PER ERN #262	6-7-82		T.J.	
D	REVISED PER ECO No 2662	7-23-82	JWC		
E	REVISED PER ECO 2677	8-17-82	D C		
F	REVISED PER ECO 2716	8-17-82	D C		

DRAWN	DATE
CHECKED	1-5-82
ENGINEER	3/1/82
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO.	NUMBER	QTY
10	0285-0154	1
	NEXT ASSEMBLY	

LIST OF MATERIAL
ASSEMBLY
ATTENUATOR BD.

biomation

B | 0285-0300 | REV R

MODEL 4500 | CODE | SHEET 1 OF 7

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19						1	1300-0007	TRANSISTOR	Q16		2N5179	
20						2	1300-0028	"	Q7,14		2N3904	
21						2	1300-0058		Q1,12		BFR96	
22						1	1400-0029		Q15		2N5208	
23						1	1500-0006	"	Q17		2N5912	
24						2	1500-0022	TRANSISTOR	Q2,8		J309	
25												
26												
27						14	2100-0007	INDUCTOR	L1,4,5,6,7,8,9,10, 13,14,15,16,17,18		10uh	
28						2	9000-0126	INDUCTOR	L2,12		TOROID 100uH	
29						4	2100-0001	INDUCTOR	L3,11,19,20		FERRITE BEAD	
30												
31						2	3300-0114	POT	R18,82		2K, 1/2W, 1T	
32												
33						5	3300-0099	POT	R28,39,74,86,	101	20K 1/2W, 1T	
34												
35						4	2950-3306	RESISTOR	R2,11,47,55		33 1/8W 5%	
36						2	2950-4706	RESISTOR	R10,54		47 1/8W 5%	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
H	REVISED PER ECO 2730	9/6/83	MW	DCW	2-14-83
J	REVISED PER ECO 2774A	9/8/83	MW	DCW	9/28
K	REVISED PER ECO 3530A	11/1/83	MW	DCW	9/24
L	REVISED PER ECO 3622	6/7/83	MW	DCW	1.583
M	REVISED PER ECO 3552	6/7/83	MW	DCW	7/5/83
N	REVISED PER ECO 3784	6/7/83	MW	DCW	7/5/83
P	REVISED PER ECO 3785	6/7/83	MW	DCW	7/5/83

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL
ASSEMBLY
ATTENUATOR BD.

biomation

B | 0285-0300 | REV R

MODEL 4500 | CODE | SHEET 2 OF 7

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
37						2	2950-1000	RESISTOR	R5,50		100 1/8W 5%	
38						3	2950-4700		R1,46,91		470 1/8W 5%	
39						2	2950-1008		R12,57		100M 1/8W 5%	
40												
41												
42						2	3100-5116		R16,79		51.1 1/8 1%	
43						2	-2000		R13,59		200	
44						2	-2430		R14,58		243	
45						2	-4990		R99,102		499	
46						4	-1001		R20,22,63,64.		1K	
47						2	-1181		R21,65		1.18K	
48						2	-1211		R25,60		1.21K	
49						2	-1241		R98,103		1.24K	
50						1	-1051		R107		1.5K	
51						1	-2001		R108		2K	
52						1	-3481		R109		3.48K	
53						4	-1002		R29,30,75,83		10K	
54						2	3100-1102	RESISTOR	R17,81		11K, 1/8W 1%	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	R	REVISED PER ECO #4143	12/2/83	[illegible]	[illegible]	[illegible]

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
ATTENUATOR BD.

biomation

B C285-0300 REV R

MODEL 4500 CODE SHEET 3 OF 7

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55						1	3100-3653	RESISTOR	R94		365K 1/8W 1%	
56						1	3100-6343		R92		634K 1/8W 1%	
57						4	3100-1004		R38,41,87,89		1M 1/8W 1%	
58												
59												
60												
61						2	9000-0096-03		R7,52		10.1K 1/8W .1%	
62						2	-05		R3,48		111K	
63						2	-04		R4,49		900KΩ	
64						2	-02		R8,53		990KΩ	
65						2	9000-0096-01		R19,56		1MΩ 1/8W .1%	
66												
67												
68												
69						4	3000-1006		R44,45,84,85		10Ω 1/4W 5%	
70						9	3000-4706		R26,37,73,80,93, 104,105,36,69		47Ω 1/4W 5%	
71						2	3000-1000		R23,67		100 1/4W 5%	
72						2	3000-3306	RESISTOR	R15,61		33Ω, 1/4W 5%	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
ATTENUATOR BD

biomation

B C285-0300 REV R

MODEL 4500 CODE SHEET 4 OF 7

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
73						4	3000-2200	RESISTOR	R9,42,70,90		220 1/4 5%	
74						2	-2700		R32,76		270	
75						8	-4700		R27,33,34,68,77 78,81,82		470	
76						2	-1001		R35,71		1K	
77						2	-1201		R40,72		1.2K	
78						1	-2201		R100		2.2K	
79						4	3000-3301		R24,43,66,88		3.3K	
80						1	3100-4992		R96		49.9K	
81						2	3000-6803		R6,51		680K	
82						2	3000-1501	RESISTOR	R110,111		1.5K 1/4 5%	
83												
84						1	4000-0027	CAPACITOR	C70		.005uf, 100V	
85						16	4000-0046		C17,25,32,33,49, 66,67,68,69,	53,59,62,65, 76-79	0.01uf, 100V, 20%	
86						6	4000-0025-10		C15,19,21,47,51 77		0.1uf, 50V, 20%	
87						2	4300-0006		C30,C55		1.0uf, 35V, 10%	
88						2	4000-0050		C22,54		.005uf, 500V	
89						3	4200-0038		C18,50,75		.068uf, 600V	
90						4	4300-0026	CAPACITOR	C24,26,58,61		15uf, 20V	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
ATTENUATOR BD.

MODEL 4500

biomation

B | 0285-0300 | REV R

CODE | SHEET 5 OF 7

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
91						2	4300-0025	CAPACITOR	C1,84		47uf, 6V, 20%	
92						2	4300-0024		C27,57		4.7uf, 50V, 10%	
93						6	4300-0013		C2,3,20,34,35, 52.		10uf, 10V, 10%	
94						2	4010-1506		C80,81		1.5pf, 50v	
95						2	4010-3306		C23,56		3.3pf, 50V	
96						2	4010-4706		C28,60		4.7pf, 100V	
97						2	4100-0016		C9,41		5pf, 500V	
98						5	4100-0005		C4,14,36,46,71		10pf, 500V	
99						2	4100-0046		C13,45		12 pf, 500V	
100						2	4100-0007		C8,40		22 pf, 500V	
101						4	4010-3306		C86-89		3.3 PF, 100V ±5%	
02						2	4000-0052		C29,63		100pf, 500V	
103						2	4000-0053		C11,43		470pf, 200V	
104						2	4000-0051	CAPACITOR	C31,64		680pf, 1000V	
105						4	4100-0017-10		C6,38,90,91		3.0pf, 500V	
106						12	4600-0018	CAP, VAR.	C5,7,10,12,16,37,39,42,44,48 73,74		0.8-6.8pf	
107						2	4010-0103	CAPACITOR	C83,85.		.01uf, 50V, 10%	
108						17	2600-0014	RELAY	K1-17			

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
ATTENUATOR BD.

MODEL 4500

biomation

B | 0285-0300 | REV R

CODE | SHEET 6 OF 7

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
109						6	7000-0607-10	SET SCREW			#8-32	
110						3	0285-0222	COAX, CABLE				
111												
112						2	6100-0019	SOCKET, I.C.	J1, 2		16 PIN	
113												
114						10	7000-0435	TERM., INSUL	E1-10			
115												
116						3	7200-0025	MOUSE TAIL			1" LONG	
117												
118						A/R	7100-0017	BUSS WIRE			22 GA.	
119												
120						3	6000-0003	CONN. BNC				
121						1	0285-0223-20	SUPPORT, BNC			ALUM. CASTING	
122						3	7000-0007	WASHER, BNC			BLACK	
123						3	7200-0039	TY WRAP MARKER				
124												
125						A/R	8300-0030-10	TAPE	C18, C50, C75		DOUBLE STICKY	
126												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
ATTENUATOR BD

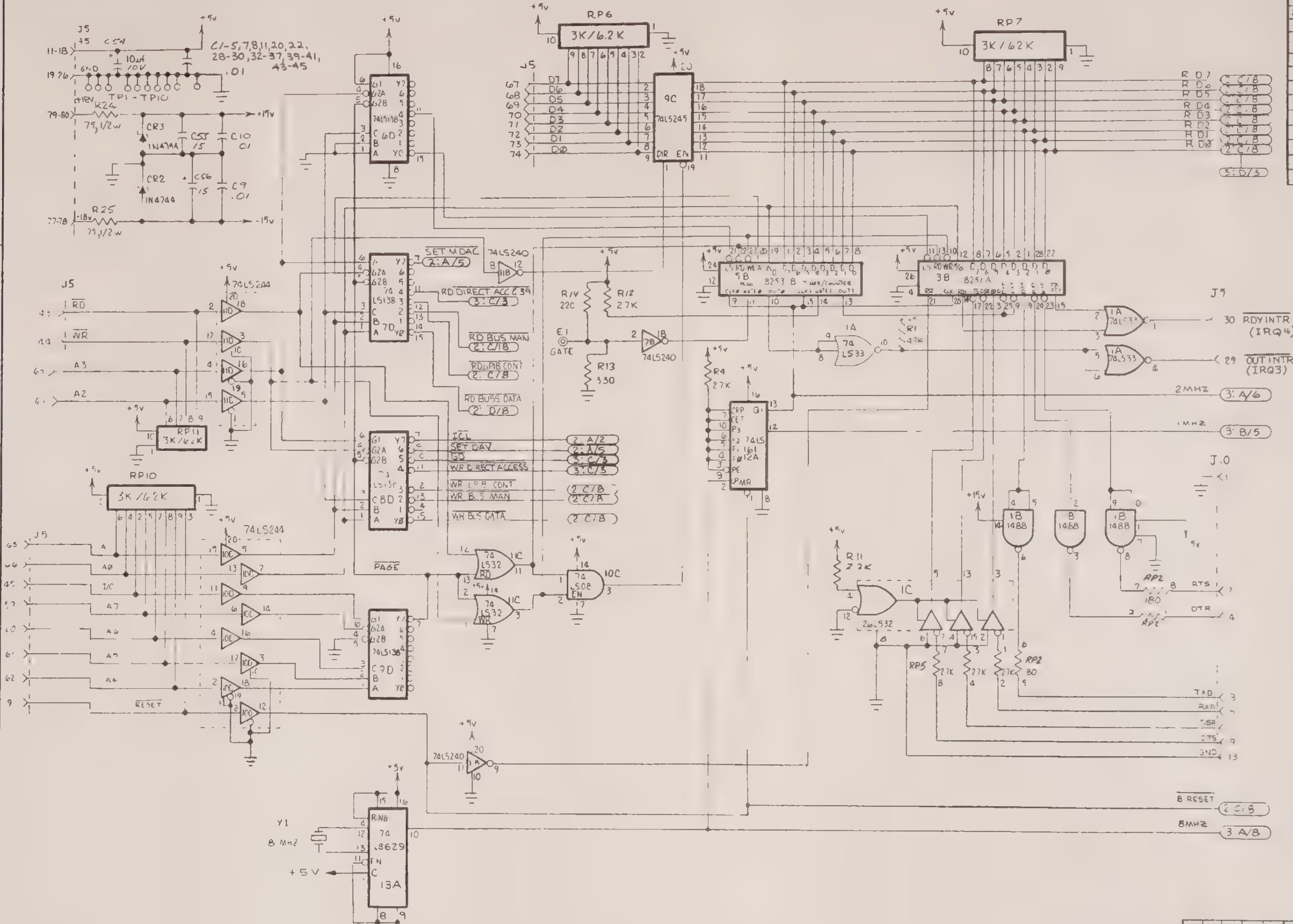
biomation

B	0285-0300	REV R

MODEL 4500 | CODE | SHEET 7 OF 7

DWG NO 0289-0061 SH 1 REV K

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PROTO TYPE	dw		3.23.81
	B		ENG UPDATE PILOT REL PER ERN № 202	DRS	RD	4/8/81
	C	2464	REVISED PER E C O N°	Sul		7/8/81
	—	2557	VOID	T.J.	T.J.	[illegible]
	D	2756	REVISED PER ECO N°	M.W.	[illegible]	11/9/81
	E	2771	REVISED PER ECO N°	MW	[illegible]	11/9/81
	E	-	PROD RELEASE PER ENR № 293	DGW	DGW	1/19/82
	—	—	REV F & G SKIPPED	mw	—	—
	H	3809	REVISED PER ECO	mw	DGW	7/29/83
	J	3558A	REVISED PER ECO	mw	DGW	7/29/83
	K	3862	REVISED PER ECO N°	SWC	DLW	9/7/83



IC TYPE	+5v PIN	GND PIN	+15 V	-15 V
26LS32	16	8	—	-
74LS02	14	7	-	—
74LS04	14	7	—	—
74LS08	14	7	—	—
74LS10	4	7	—	-
74LS33	14	7	—	-
74LS74	4	7	—	-
74LS122	14	7	—	-
74LS629	16	8	—	—
74LS138	16	8	—	—
74LS161	16	8	—	—
74LS191	16	8	—	—
74LS244	20	10	—	—
74LS245	20	10	—	-
74LS273	20	10	—	—
74LS374	20	10	—	—
1488	—	7	14	1
7681	24	12	-	-
8251	26	4	-	-
8253	24	12	—	-
NE5018	—	1	19	17
74LS160	16	8	—	-
74LS107	14	7	—	-
74LS20	4	7	—	-
74LS266	14	7	—	-
74LS240	20	10	-	-
74LS112	16	8	—	-
7438	14	7	-	-
74LS32	14	7	-	-
74LS0?	14	7	—	-
74LS30	4		—	—

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITOR ARE IN MICROFARADS.

DASH NO	NUMBER (NEXT ASSEMBLY)	QTY
-10	0285-0060	1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

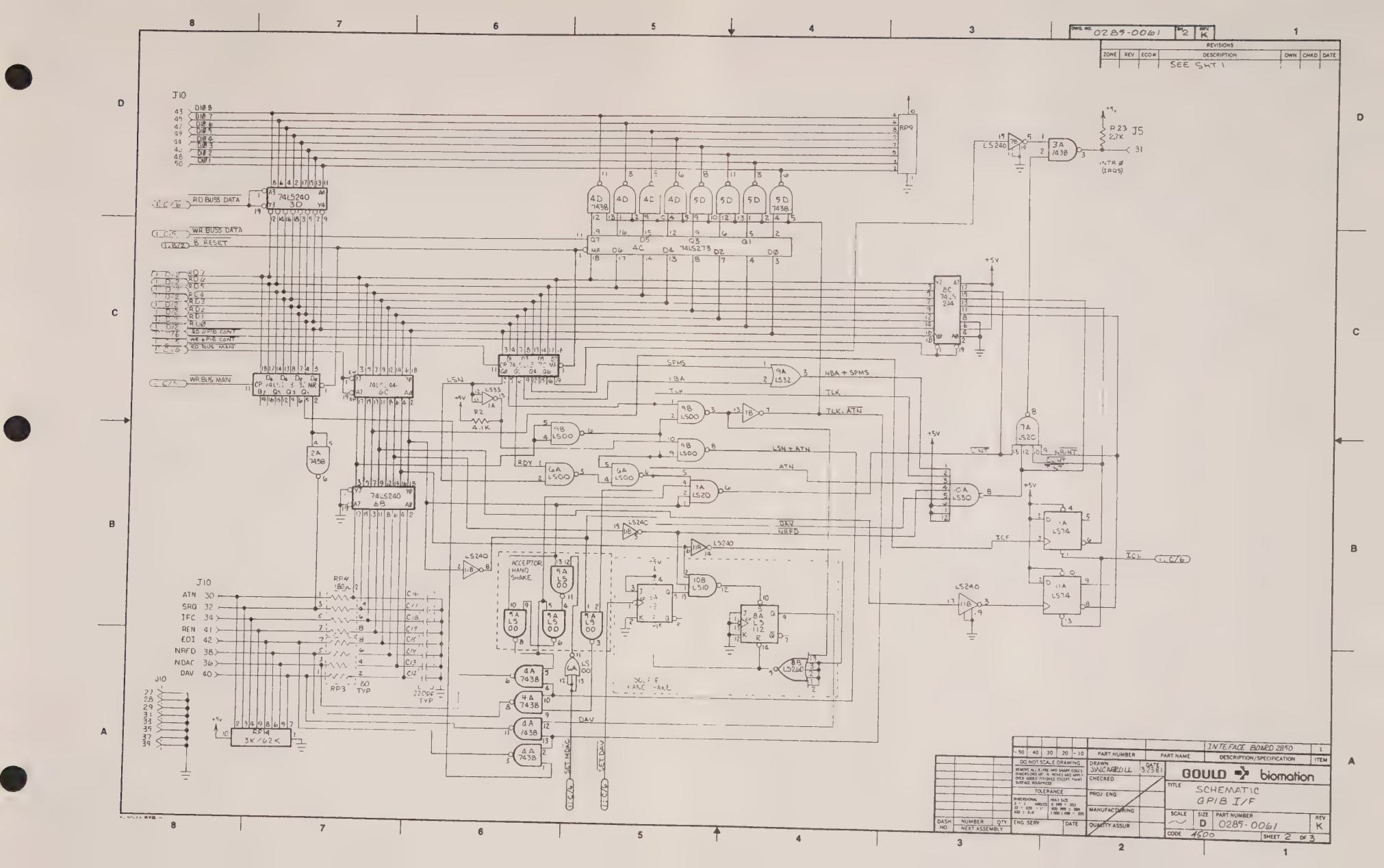
DRAWN: J. W. CARROLL — DATE 3.23.81
CHECKED: [signature] — 4-8-81
PROJ ENG
MANUFACTURING: [signature]
QUALITY ASSUR: [signature] — 1-82
ENG SERV — DATE

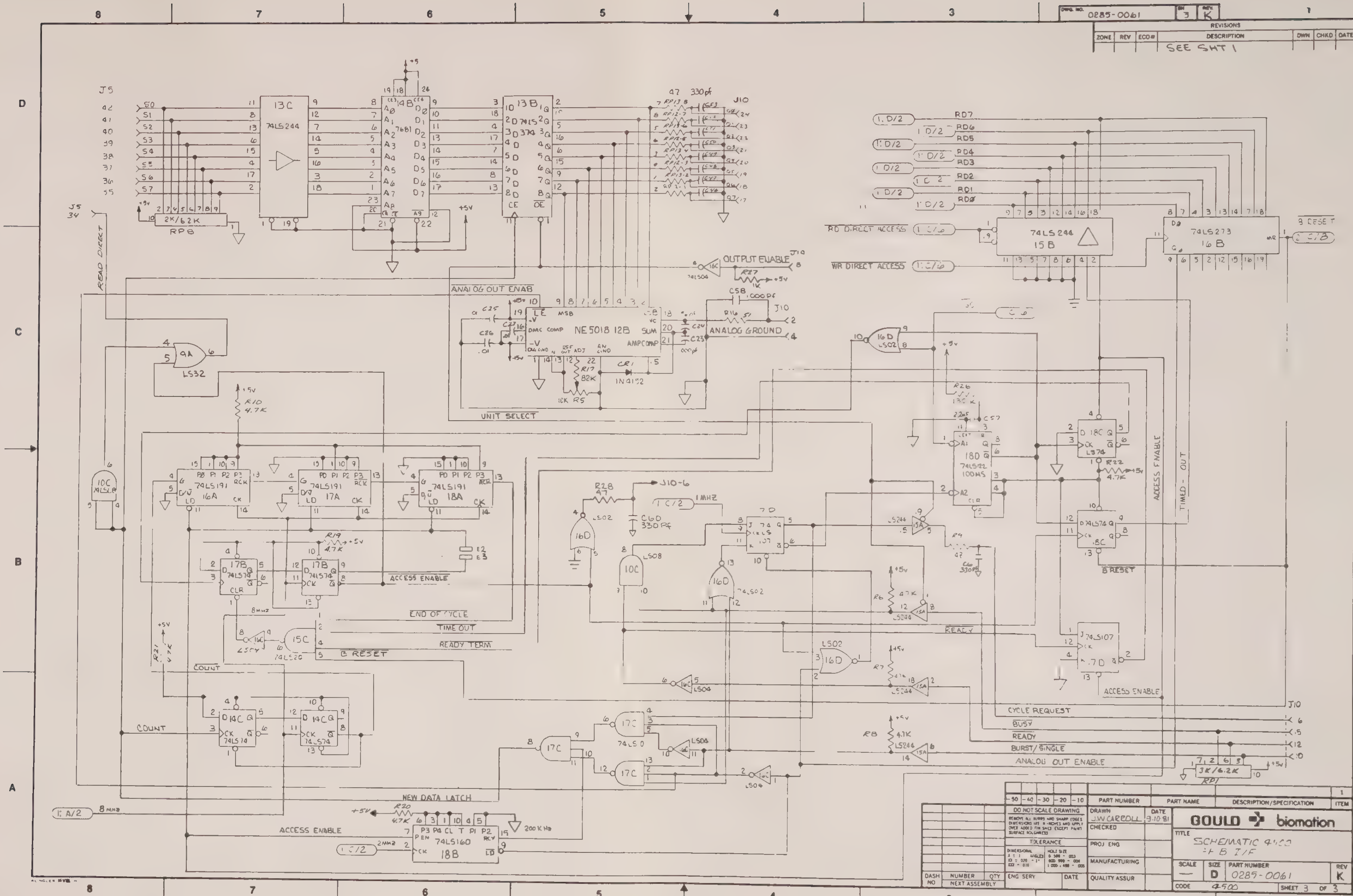
GOULD biomation

TITLE: SCHEMATIC GPIB I/F

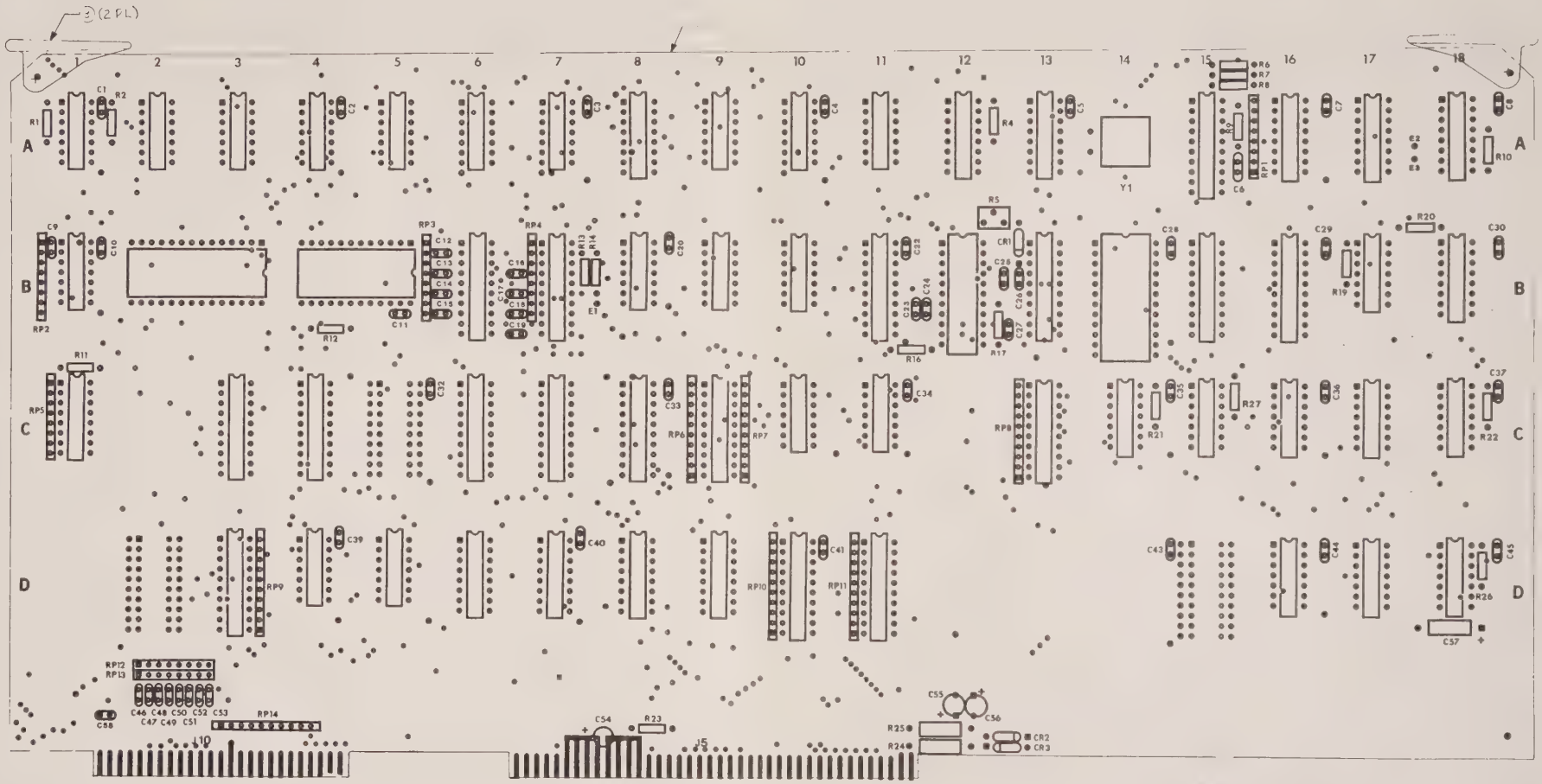
SCALE: ~ | SIZE: D | PART NUMBER: 0285-0061 | REV: K

CODE 4500 | SHEET 1 OF 3


DWG. NO. 0289-0061
REV K
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
J10
RD BUSS DATA
WR BUSS DATA
B RESET
WR BUS MAN
74LS240
74LS273
74LS244
LS240
LS32
LS00
LS20
LS30
LS74
LS10
LS112
LS14
RP9
RP4
RP14
3K/62K
R23 2.7K
J5
R2 4.1K
+5V
LSN
SPMS
TLK
RDY
ATN
NRFD
NDAC
DAV
IFC
REN
EOI
SRQ
ATN
ACCEPTOR HAND SHAKE
SET NDAC
SET DAV
INTERFACE BOARD 2850
GOULD biomation
SCHEMATIC GPIB I/F
SIZE D
PART NUMBER 0289-0061
REV K
CODE 1500
SHEET 2 OF 3


0285-0061
SH 3
REV K
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
SEE SHT 1
J5
74LS244
13C
14B
13B
74LS374
NE5018 12B
ANALOG OUT ENAB
UNIT SELECT
OUTPUT ENABLE
ANALOG GROUND
J10
RD DIRECT ACCESS
WR DIRECT ACCESS
74LS244 15B
74LS273 16B
B RESET
READ DIRECT
LS32
74LS191 16A
74LS191 17A
74LS191 18A
ACCESS ENABLE
END OF CYCLE
TIME OUT
READY TERM
B RESET
COUNT
74LS123
74LS74
74LS107
CYCLE REQUEST
BUSY
READY
BURST/SINGLE
ANALOG OUT ENABLE
NEW DATA LATCH
74LS160 18B
200 KHz
1 MHZ
8 MHz
2 MHz
TIMED-OUT
ACCESS ENABLE
DO NOT SCALE DRAWING
DRAWN J.W. CARROLL 9-10-81
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
TOLERANCE
GOULD biomation
TITLE SCHEMATIC 4500 GPIB I/F
SCALE
SIZE D
PART NUMBER 0285-0061
REV K
CODE 4500
SHEET 3 OF 3
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	—	—	[illegible]			
	H	[illegible]	REVISED [illegible]			
	[illegible]	[illegible]	REVISED [illegible]			
	K	38862	REVISED PER ECO NO	JWK	DGW	8-29-89
		42816	REVISED PER ECO NO	JWC	DGW	8/29/89



NOTES: UNLESS OTHERWISE SPECIFIED

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY
OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 ± 1°; XXX = .010
HOLE SIZE: 0.599 - .003; .000 .999 - .004; 1.000 1.499 - .005

DRAWN	DATE
CHECKED	
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR	

GOULD biomation

TITLE

SCALE	SIZE	PART NUMBER	
	D		L

CODE 45 SHEET OF

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG SERV DATE

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
37						10	3000-4701	RESISTOR	R1,2,6,7,8,10, 19-22		4.7K, 1/4W, 5%	
38						3	-2701		R4,12,23		2.7K	
39						1	-2200		R14		220Ω	
40						1	-4706		R9		47Ω	
41						1	-2201		R11		2.2K	
42						1	-3300		R13		330Ω	
43						1	-5106		R16		51Ω	
44						1	-8202		R17		82K	
45						1	3000-1303		R26		130K, 1/4W, 5%	
46						2	3050-7506	RESISTOR	R24,25		75Ω, 1/2W, 5%	
47						1	3000-1001	"	R27		1K, 1/4W 5%	
48						1	3300-0024	RES. VAR.	R5		10K, 1 TURN	
49						29	4010-0103	CAPACITOR	C1-5,7-11,20,22, 25-30,32-37,39-41, 43-46		.01 µf, 50V	
50												
51						10	-0331		C6,46-53,60		330 pf, 100V	
52						1	-0560		C24		56 pf, 100V	
53						2	4010-0102-10	CAPACITOR	C23,58		1000 pf, 100V	
54												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
S. RODELL	9-10-81
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO. | NUMBER | QTY | NEXT ASSEMBLY

LIST OF MATERIAL
ASSEMBLY,
GPIB INTERFACE BD.

MODEL 4500

biomation

B | 0285-0060 | REV K

CODE | SHEET 3 OF 4

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55						11	4300-0013	CAPACITOR	C54		10 µf 10V	
56						2	4300-0015	CAPACITOR	C55,56		15 µf	
57						1	4300-0012	CAPACITOR	C57		2.2 µf 35V	
58						8	4010-0221	CAPACITOR	C12-19		220pf 100V	
59						1	1000-0002	DIODE	CR1		IN 4152	
60						2	1100-0027	DIODE	CR2,3		IN 4744	
61												
62						1	3700-0088	RES PAK	RP1		3K/6.2K, 8 PIN	SIP
63						3	-0056		RP2,3,4		180Ω, 8 PIN	
64						1	-0084		RP5		2.7K, 8 PIN	
65						7	-0049		PR6-11,14		3K/6.2K, 10 PIN	
66						2	3700-0076	RES PAK	RP12,13		47Ω 8 PIN	SIP
67						1	5100-0001	CRYSTAL	Y1		8 MHZ	
68						1	6100-0151	SOCKET	3B		28 PIN DIP,LP	
69						1	6100-0136	"	12B		22 PIN	
70						2	6100-0122	SOCKET	14B,5B		24 PIN DIP,LP	
71						10	0285-0311	TEST POINT	TP1-10			
72												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
S. RODELL	3-10-81
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO | NUMBER | QTY | NEXT ASSEMBLY

LIST OF MATERIAL
ASSEMBLY,
GPIB, INTERFACE BD.

MODEL 4500

biomation

B | 0285-0060 | REV K

CODE | SHEET 4 OF 4

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0285-0062	P.C.B.				FAB
2												
3						2	7000-0120	EJECTOR				
4												
5						3	1800-0105	I.C.	5A, 6A, 9B		74 LS 00	
6						1	-0109		10C		74 LS 08	
7						2	-0110		10B, 17C		74 LS 10	
8						2	-0216		9A, 11C		74 LS 32	
9						1	-0347		1A		74 LS 33	
10						5	-0311		2A, 3A, 4A, 4D, 5D		7438	
11						1	-0068		8A		74 LS 112	
12						1	-0357		13A		74 LS 629	
13						1	-0125		12A		74 LS 161	
14						4	-0267		6B, 7B, 11B, 3D		74 LS 240	
15						7	-0240		6C, 8C, 10D, 11D, 13C, 15A, 15B		74 LS 244	
16						1	-0268		9C		74 LS 245	
17						1	-0309		8B		74 LS 260	
18						2	1800-0111	I.C.	7A, 15C		74 LS 20	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
G	REVISED PER ECO No 3570	7-16	DGW	[illegible]	
H	REVISED PER ECO No 3809	5/24/83	MW	DGW	7/29/83
J	REVISED PER ECO NO 3558 A	7/29/83	MW	DGW	7/29/83
K	REVISED PER ECO N° 3862	8/29/83	[illegible]	DGW	8/31/83

DASH NO.	NUMBER	QTY
-10	0285-0002	1
NEXT ASSEMBLY		

DRAWN B. RIDDELL 9-10-81
CHECKED
ENGINEER
MANUFACTURING 11-11-82
QUALITY ASSURANCE 11-11-82

LIST OF MATERIAL
ASSEMBLY,
GPIB, INTERFACE BD.

biomation

B 0285-0060 REV K

MODEL 4500 CODE SHEET 1 OF 4

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19						4	1800-0115	I.C.	11A, 14C, 17B, 18C		74 LS 74	
20						3	-0247		16A, 17A, 18A		74 LS 191	
21						4	-0231		16B, 3C, 4C, 7C		74 LS 273	
22						1	-0107		16C		74 LS 04	
23						1	-0106		16D		74 LS 02	
24						1	-0182		17D		74 LS 107	
25						1	-0221		18B		74 LS 160	
26						1	-0293		13B		74 LS 374	
27						1	-0343		3B		8251A	
28						1	1800-0344		5B		8253B	
29						1	1800-0188		10A		74LS30	
30						1	1900-0013		12B		NE5018	
31												
32						1	1800-0331		14B		7681	
33						1	1800-0354		18D		74 LS 122	
34						1	1700-0101		1B		1488	
35						1	1700-0102	I.C.	1C		26 LS 32	
36						4	1800-0193	I.C.	6D, 7D, 8D, 9D		74LS138	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
NEXT ASSEMBLY		

DRAWN B. RIDDELL 9-10-81
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
ASSEMBLY,
GPIB INTERFACE BD.

biomation

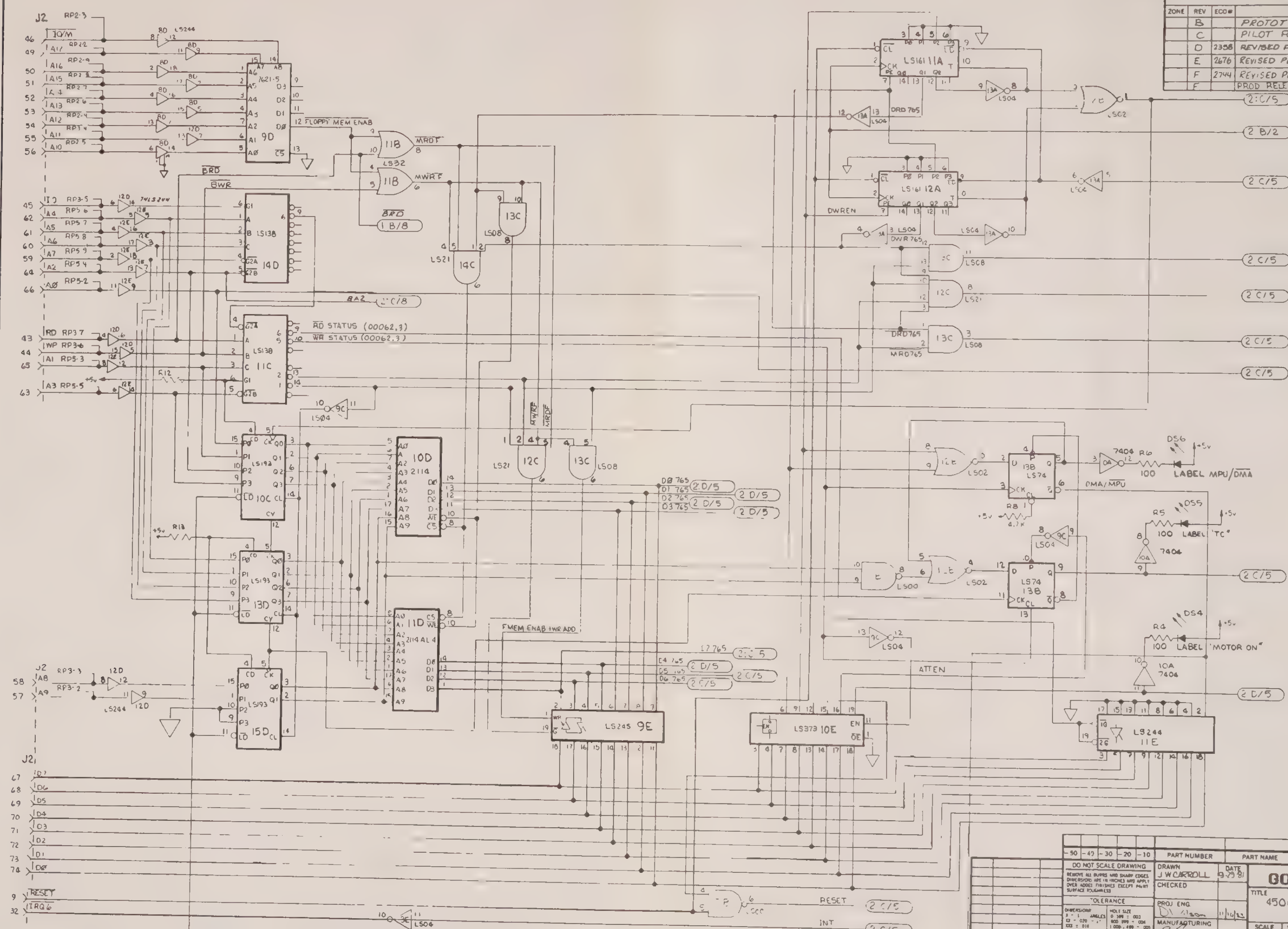
B 0285-0060 REV K

MODEL 4500 CODE SHEET 2 OF 4

DWG. NO	SH	REV
0285-0056	1	J

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	B		PROTOTYPE	—	RD	10/9/81
	C		PILOT REL ERN # 221	BH.	RG	1/11/82
	D	2358	REVISED PER ECO No	JWC	RD	3/10/82
	E	2676	REVISED PER ECO	RER	[illegible]	10/22/[illegible]
	F	2744	REVISED PER ECO	RER	[illegible]	10/22/[illegible]
	F		PROD RELEASED PER ERN 0288			



I C	Vcc	GND
7621-5	16	8
LS138	16	8
LS193	16	8
2114 AL-4	18	9
LS245	20	10
LS161	16	8
LS373	20	10
LS244	20	10
LS74	14	7
8272	40	20
74LS174	16	8
LS629	16	8
2764	28	14
74LS32	14	7
LS157	16	8
LS02	14	7
LS04	4	7
LS08	14	7
LS21	14	7
LS00	14	7

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DASH NO | NUMBER | QTY — NEXT ASSEMBLY

ENG SERV | DATE

DRAWN J W CARROLL — DATE 9-29-81

CHECKED

PROJ ENG — 11/16/82

MANUFACTURING — 11/1/82

QUALITY ASSUR — 11-1-82

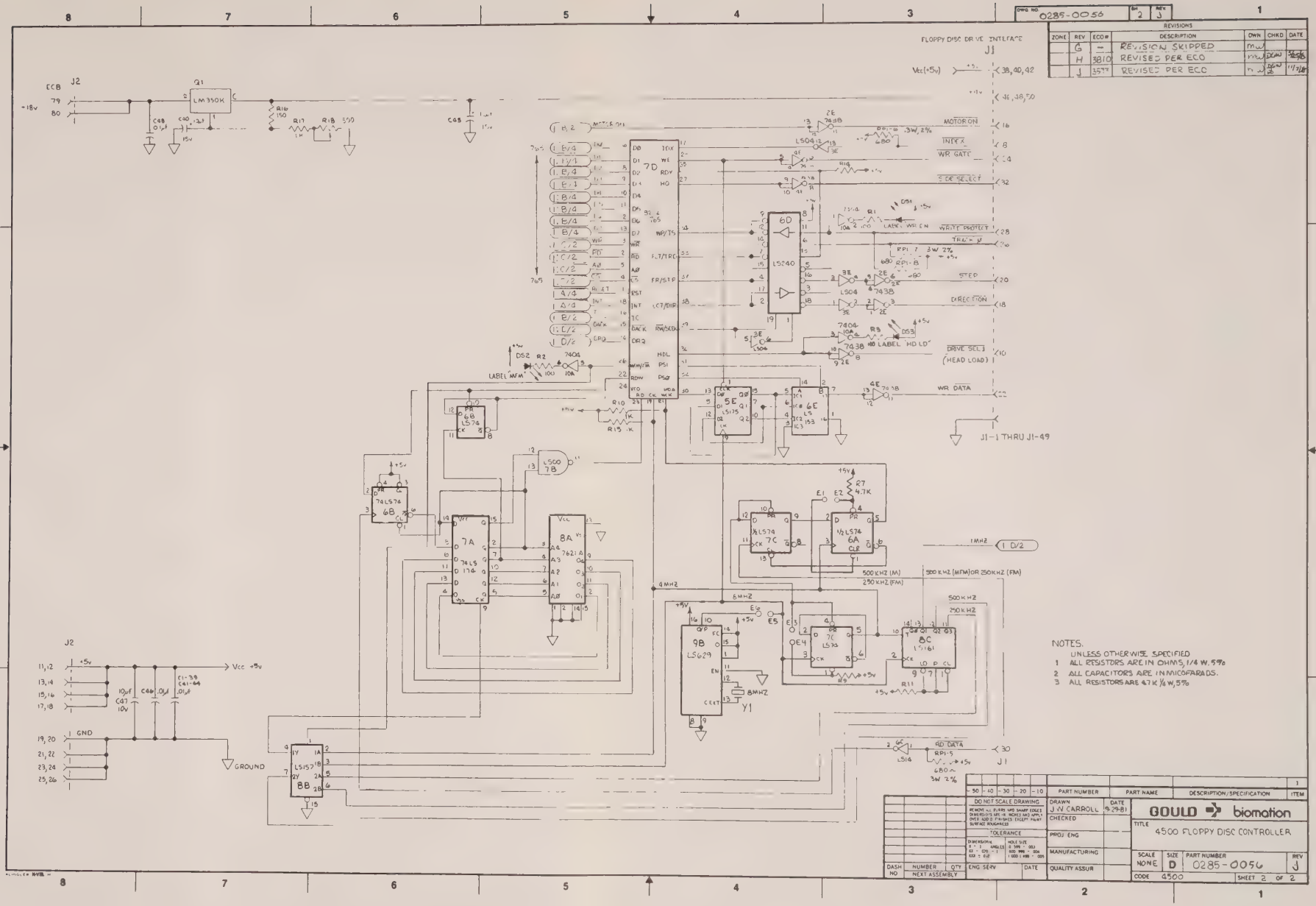
GOULD biomation

TITLE 4500 FLOPPY DISC CONTROLLER

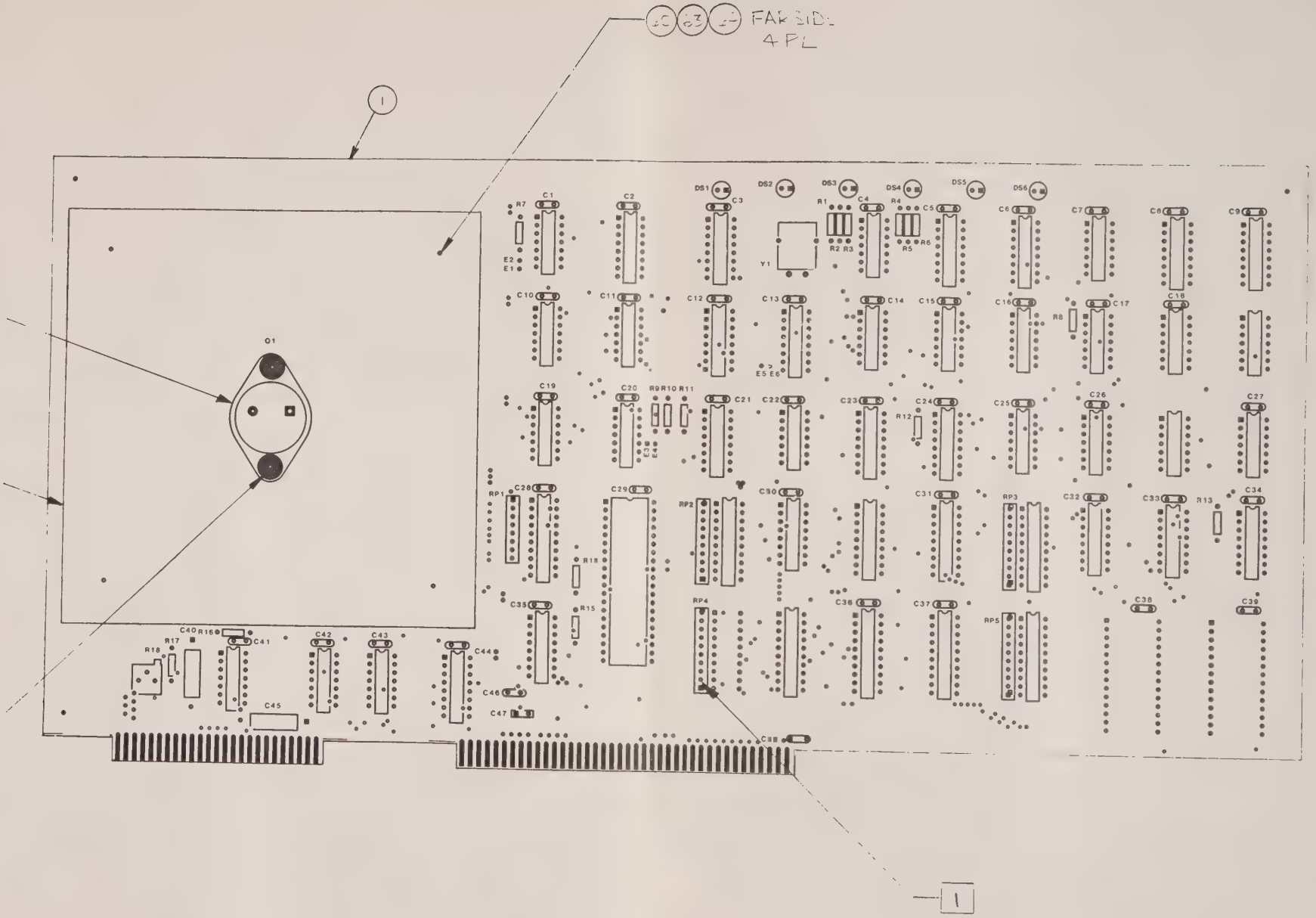
SCALE NONE | SIZE D | PART NUMBER 0285-0056 | REV J

CODE

SHEET 1 OF 2



DWG NO 0285-0056
SH 2
REV J
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
G | — | REVISION SKIPPED | mw
H | 3810 | REVISED PER ECO | mw | DCW
J | 3577 | REVISED PER ECO | mw | DCW
FLOPPY DISC DRIVE INTERFACE
J1
Vcc(+5v)
38, 40, 42
46, 48, 50
MOTOR ON
INDEX
WR GATE
SIDE SELECT
WRITE PROTECT
TRACK
STEP
DIRECTION
DRIVE SEL 1 (HEAD LOAD)
WR DATA
J1-1 THRU J1-49
LABEL "WR EN"
LABEL "HD LD"
LABEL "MFM"
7D
6D
LS240
5E
LS175
6E
LS153
6B
LS74
LS00
7B
7A
74LS174
8A
7621
6A
½LS74
7C
9B
LS629
8C
LS161
LS157
8B
LS14
Y1
8MHZ
4MHZ
8MHZ
1MHZ
1 D/2
500 KHZ (M)
250 KHZ (FM)
500 KHZ (MFM) OR 250 KHZ (FM)
500 KHZ
250 KHZ
RD DATA
J2
ECB
+18v
Q1
LM350K
GND
GROUND
Vcc +5v
NOTES.
UNLESS OTHERWISE SPECIFIED
1 ALL RESISTORS ARE IN OHMS, 1/4 W. 5%
2 ALL CAPACITORS ARE IN MICOFARADS.
3 ALL RESISTORS ARE 47 K 1/4 W, 5%
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN J W CARROLL
DATE 9-29-81
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE 4500 FLOPPY DISC CONTROLLER
SCALE NONE
SIZE D
PART NUMBER 0285-0056
REV J
CODE 4500
SHEET 2 OF 2


FAR SIDE
4 PL
1
Q1
DS1
DS2
DS3
DS4
DS5
DS6
Y1
R1
R2 R3
R4
R5
R6
R7
R8
R9 R10 R11
R12
R13
R15
R16
R17
R18
E1
E2
E3
E4
E5 E6
C1
C2
C3
C4
C5
C6
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C13
C14
C15
C16
C17
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C19
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C23
C24
C25
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C28
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C30
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
RP1
RP2
RP3
RP4
RP5
1

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
37						2	6100-0120	SOCKET	X8A, X9D		16 PIN	
38						2	6100-0156	SOCKET	X10D, X11D		18 PIN	
39												
40												
41												
42						7	3000-4701	RESISTOR	R7,8,9, 11-14		4.7K 1/4W, 5%	
43												
44						6	3000-1000	RESISTOR	R1-6		100Ω, 1/4W, 5%	
45												
46						1	-1500		R16		150, 1/4W, 5%	
47												
48						3	-1001		R10, 15, 17		1K, 1/4W, 5%	
49												
50												
51						1	3700-0052	RES PACK	RP1		680Ω .3W 2%	
52						3	3700-0049	RES PACK	RP2-3,5		3K/6.2K 10 PIN	
53						1	3300-0037	POT	R18		500 Ω	
54						1	0285-0205	HEAT SINK				

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
J. PERGINS	1/7/81
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL

FLOPPY DISK I/F PWB

MODEL 4500

biomation

B 0285-0055 REV J

CODE

SHEET 3 OF 4

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55						2	4400-0039	CAPACITOR	C40 C45		ELECT 10uf 15V	
56						1	4300-0013		C47		ELECT 10uf 10V	
57						1	4000-0025		C48		CERAMIC .01uf	
58						14	4000-0044	CAPACITOR	C1-39 41-44, 46		CERAMIC 0.01uf 100V	
59												
60						4	7011-1632-08	SCREW			#6-32 x 1/4	
61						2	7011-1632-16	SCREW			#6-32 x 1/2	
62						2	7070-1632-00	NUT			#6-32	
63						6	7080-1006-00	WASHER			#6	
64						4	7083-1006-00	LOCK WASHER			#6	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
J. PERGINS	1/7/81
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL

FLOPPY DISK I/F PWB

MODEL 4500

biomation

B 0285-0055 REV J

CODE

SHEET 4 OF 4

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0285-0057	PWB				
2						1	1800-0342	I.C.	7D		8272	
3						2	1800-0257		10D, 11D		2114-AL-4	
4												
5						1	1800-0005		10A		SN7404	
6						2	-0311		2E, 4E		SN7438	
7						3	-0107		3E, 9C, 13A		SN74LS04	
8						1	-0123		6C		SN74LS14	
9						1	0105		7B		SN74LS00	
10						1	-0106		12B		SN74LS02	
11						1	-0109		13C		SN74LS08	
12						2	-0275		12C, 14C		SN74LS21	
13						1	-0216		11B		SN74LS32	
14						4	-0115		6B, 7C, 13B 6A		SN74LS74	
15						3	-0125		8C, 11A, 12A		SN74LS161	
16						1	-0213		8B		SN74LS157	
17						1	-0357		9B		SN74LS629	
18						1	1800-0181	I.C.	5E		SN74LS175	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
B	PROTOTYPE	10/6/81	KL		
C	PILOT REL ERN # 221	11-7-82	B.H		
D	REVISED PER ECO # 2358	8-10-82	JWC	RD	
E	REVISED PER ECO # 2580	3-10-82	JWC		
F	REVISED PER ECO # 2676	10-7-82	BH		
G	REVISED PER ECO # 2744	10-7-82	BH		
G	PROD RELEASED PER ERN. 0288	11-4-82	DLWC	—	—

DASH NO	NUMBER	QTY
-10	0285-0135	1
NEXT ASSEMBLY		

	DRAWN	DATE
	J. PERGINS	1/7/81
	CHECKED	
	ENGINEER	
	MANUFACTURING	11-4-82
	QUALITY ASSURANCE	11-4-82

LIST OF MATERIAL
FLOPPY DISK I/F
PWB

MODEL 4500

biomation

B | 0285-0055 | REV J

CODE | SHEET 1 OF 4

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19						1	1800-0217	I.C.	6E		SN74LS153	
20						1	-0267		6D		SN74LS240	
21						2	-0193		11C, 14D		SN74LS138	
22						3	-0134		10C, 13D, 15D		SN74LS193	
23						4	-0240		8D, 11E, 12E, 12D		SN74LS244	
24						1	-0268		9E		SN74LS245	
25						1	-0298		10E		SN74LS373	
26						1	1800-0190		7A		SN74LS174	
27						2	1800-0322	I.C.	9D, 8A		7621	
28						1	1700-0109		Q1		LM355K	
29						1	7200-0016	INSULATOR	Q1			
30												
31												
32												
33						6	6400-0039	LED, RED	DS1-6			
34						1	5100-0001	CRYSTAL	Y1		8MHZ	
35						1	6100-0123	SOCKET	X7D		40 PIN	
36												

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
H	REVISED PER ECO 3810	5/24/83	MJ	JWC	5/26/83
J	REVISED PER ECO 3573	10/9/83	MJ	JWC	10/12/83

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	J. PERGINS	1/7/81
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL
FLOPPY DISK I/F
PWB

MODEL 4500

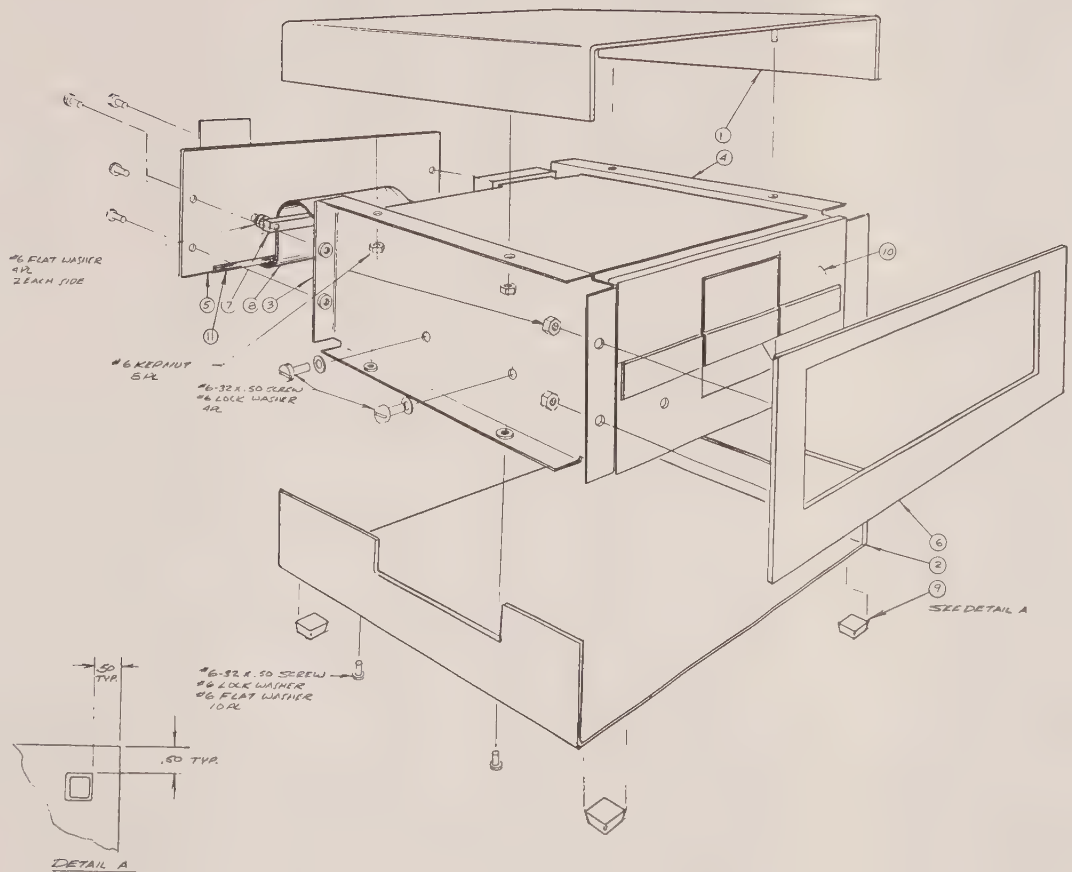
biomation

B | 0285-0055 | REV J

CODE | SHEET 2 OF 4

DWG NO. 0295-0296 | SH 1 | REV C

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL PER E.C.N.K. 221	DRS	RG	7/1/81
	B	2946	REVISED PER E C O	DWC		7-18-82
	C	3650	REVISED PER ECO	MW	DW	4/13/83



DASH NO	NEXT ASSEMBLY NUMBER	QTY
-10	0295-0297	1

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

TOLERANCE

ENG SERV | DATE

DRAWN	SANDELL	12-18-81
CHECKED	DW	1-14-83
PROJ ENG	DRS	1-6-83
MANUFACTURING		1/4/83
QUALITY ASSUR		1/4/83

GOULD biomation

TITLE FLOPPY TOP ASSY

SCALE	SIZE	PART NUMBER	REV
NONE	D	0295-0296	C

CODE 4500 | SHEET 1 OF 1

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0285-0290	TOP COVER				
2						1	-0291	LOWER COVER				
3						1	-0292-10	SIDE BRACKET LEFT				
4						1	-0292-20	SIDE BRACKET RIGHT				
5						1	-0293	REAR PNL				
6						1	-0294	FNT PNL				
7						1	-0295	CLAMP				
8						1	0285-0305	CABLE ASSY				LM
9						4	7000-0243-10	HDWR RUBBER BUMPER 9/16				
10						1	7500-0002	DISK DRIVE				
11						A/R	7200-0044	FLEX GROMMET SPEC-2 ROLL			5.60 LONG	
12												
13												
14												
15												
16												
17												

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL PER ERN NO 221	12-8-82	DRS	DGW	
B	REVISED PER ECO NO 2546	1-14-83	DWC	DGW	
C	REVISED PER ECO # 3650	4/12/83	MW		

DASH NO.	NEXT ASSEMBLY NUMBER	QTY
-10	0285-0297	1

		DATE
DRAWN	JANDELL	12-8-81
CHECKED	DGW	1-14-83
ENGINEER	DRS	1-6-83
MANUFACTURING		1/6/83
QUALITY ASSURANCE		1/6/83

LIST OF MATERIAL

FLOPPY TOP ASSY

biomation

B	0285-0296	REV C

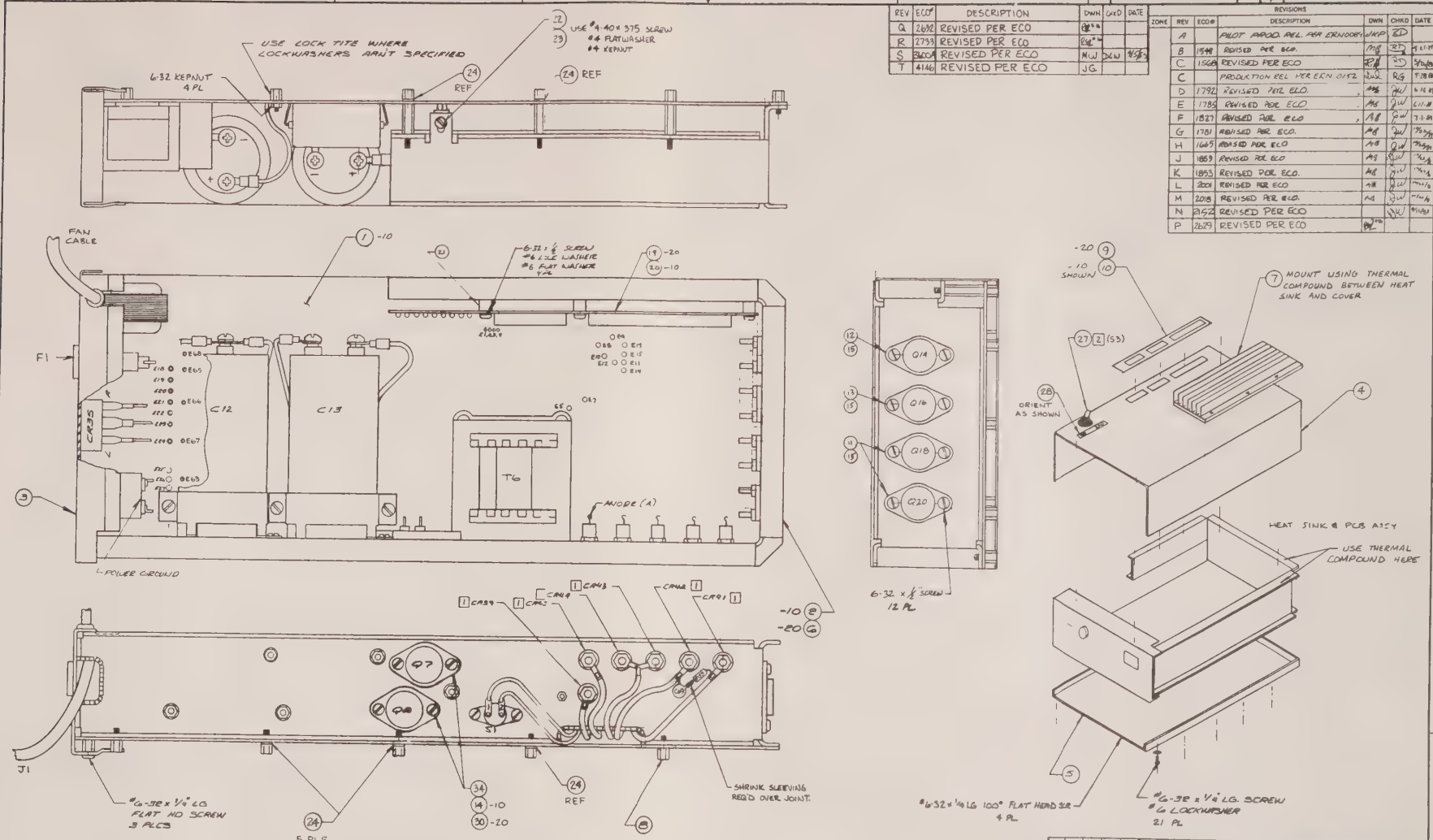
MODEL 4500 | CODE | SHEET 1 OF 1

DWG NO 0285-0003 SH 1 REV T

REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
Q	2692	REVISED PER ECO	[illegible]		
R	2733	REVISED PER ECO	[illegible]		
S	3600A	REVISED PER ECO	MW	DCW	4/5/83
T	4146	REVISED PER ECO	JG		

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT PROD. REL. PER ERN0084	JKP	RD	
	B	1548	REVISED PER ECO.	MG	RD	5-21-81
	C	1568	REVISED PER ECO	[illegible]	RD	5/28/81
	C		PRODUCTION REL PER ERN 0152	[illegible]	RG	7-28-81
	D	1792	REVISED PER ECO.	MG	JW	6-16-81
	E	1785	REVISED PER ECO	MG	JW	6-11-81
	F	1827	REVISED PER ECO	MG	JW	7-1-81
	G	1781	REVISED PER ECO.	MG	JW	10/22/81
	H	1665	REVISED PER ECO	MG	JW	10/29/81
	J	1859	REVISED PER ECO	MG	JW	10/22/81
	K	1853	REVISED PER ECO.	MG	JW	10/22/81
	L	2001	REVISED PER ECO	MG	JW	10/22/81
	M	2018	REVISED PER ECO.	MG	JW	10/22/81
	N	2152	REVISED PER ECO		JW	9/15/81
	P	2629	REVISED PER ECO	[illegible]		



DASH NO	NUMBER NEXT ASSEMBLY	QTY
-20	0285-0019	1
-10	0114-0003	1
-10	0950-0003	

DO NOT SCALE DRAWING

TOLERANCE

ENG SERV RG DATE 5/29/81

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DRAWN J. PERGINS DATE 4/8/81
CHECKED RG 5/29/81
PROJ ENG 6/5/81
MANUFACTURING 6/3/81
QUALITY ASSUR 6/3/81

GOULD biomation

TITLE TOP ASSEMBLY POWER SUPPLY

SCALE | SIZE D | PART NUMBER 0285-0003 | REV T

CODE 4500 | SHEET 1 OF 2

DWG. NO 0285-0003 SH 2 REV T

REVISIONS

ZONE	REV	ECO #	DESCRIPTION	OWN	CHKD	DATE

WIRE LIST

WIRE Nº	FROM	TO	DESCRIPTION
1	E1 FILTER PWB	E1 PS PWB	BRN
2	E2	E2	RED
3	E7	E7	ORG
4	E9	C9	YEL (18)
5	E5	E5	LT BLU
6	—	—	—
* 7	E14	E7	VIO
8	E6	E8	BRN
9	E7	E9	RED
10	E13	E10	ORG (17)
11	E8	E11	YEL
12	E9	E12	LT BLU
13	E10	E13	BRN
14	E11	E14	RED (16)
15	E12	E15	ORG
16	E16 PS PWB	S1-1 HEAT SINK	BRN
17	E17 PS PWB	S1-3 "	RED
18	E15 FILTER BD.	E70 P.S. PWB	VIO
20	E20 P.S. PWB.	CR35 (-)	BLK
21	E21	" (-)	VIO
22	C22	" (+)	YEL
23	E23	" (R)	ORG
24	—	—	—
25	J1-2 FACE PLATE	E25 PS PWB	WHT BRN
26	E26 PS PWB	PWR GND	GRN/YEL
27	J1-4 FACE PLATE	E27 PS. PWB	BLK/BLU
28	E28 PS PWB	C12 (-) HEAT	RED
29	E29	C12 (+) SINK	BRN
30	E30	C13 (-) "	RED
31	E31	C17 (+) "	BRN
39	T6	CR42 (C) HEAT	BLK [3]
39	E39	CR40 (C) SINK	ORG
40	E57	CR47 (A)	ORG
41	E40	CR39 (C)	RED
42	E60	CR49 (A)	RED
43	T6	CR41 (C)	BLK [3]
44	E42	CR39,40 (A)	BRN
45	E43	CR41,42 (A)	YEL
46	E44	CR43,44 (C)	WHT/RED
G1	E61	S1-NO	BRN
G2	E62	S1-COM	RED

* -20 ONLY

S3 WIRE LIST AND DETAIL [2]

WIRING LIST FROM	TO
S3-1	E66
S3-2	E65
S3-3	S3-6
S3-4	E63
S3-5	E64
S3-7	E68
S3-8	E67

NOTES:

[1] SOLDER LUGS ON DIODES TO HAVE A MIN. OF .100 CLEARANCE TO HEAT SINK & TOP COVER.

[2] WIRES TO BE 7-10 INCHES LONG TO ALLOW FOR SERVICE LOOP. SHRINK TUBE ALL CONNECTIONS AT S3 TO PREVENT SHORTS.

[3] BLACK WIRES FROM T6 ARE INTERCHANGABLE.

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG. SERV — DATE

DO NOT SCALE DRAWING

TOLERANCE

DRAWN — DATE

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

PART NUMBER | PART NAME | DESCRIPTION/SPECIFICATION | ITEM

GOULD biomation

TITLE TOP ASSEMBLY POWER SUPPLY

SCALE NONE | SIZE D | PART NUMBER 0285-0003 | REV T

CODE | SHEET 2 OF 2

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1												LM
2												LM
3					1		0285-0156	FACE PLATE ASSY				LM
4					1		0285-0175	TOP COVER				
5					1		0285-0174	LOWER COVER				
6					1		0285-0173-20	HEAT SINK ASSY				LM
7											TOP	FAB
8					14		7000-0423	M/F STANDOFF				
9					1		0285-0203-20	LABEL 4500				
10												
11					2		1400-0039	TRANSISTOR	Q18,20	2N4276		
12					1		1300-0042	"	Q 14	2N5885		
13					1		1400-0030	"	Q 16	2N5883		
14												
15					6		7200-0016	INSULATOR	Q7,8,14,16,18,20	60-11-4996-1666		
16												LM
17												LM
18												LM

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
P	REVISED PER ECO 2029	8/24	[illegible]	DWN	
Q	REVISED PER ECO 2032	8/28	KSH	DWN	
R	REVISED PER ECO 2733	11-1782	KSH	DWN	
S	REVISED PER ECO 3666CA	3/29/83	MW	DWN	4/5/83
T	REVISED PER ECO 4146			JG	
E	REVISED PER ECO # 1785	6/18	MZ		
F	REVISED PER ECO # 1827	7/8	MZ		

DASH NO	NUMBER NEXT ASSEMBLY	QTY
-80	0285-0019	1
-10	0114-0003	1
-10	0950-0003	1

	DATE
DRAWN J. PERGINS	6/30/80
CHECKED RG	5/26/81
ENGINEER	
MANUFACTURING	6/3/81
QUALITY ASSURANCE	6/3/81

LIST OF MATERIAL
POWER SUPPLY
TOP ASSEMBLY

biomation

B | 0285-0003 | REV T

MODEL 4500 | CODE | SHEET 1 OF 2

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19					1		0285-0180	FILTER BOARD				LM
20												LM
21					4		7000-0022	SPACER 1/4 #6				
22					1		7000-0319	SHOULDER WASHER	Q1		#4	
23					1		7000-222-10	INSULATOR	Q1			
24					5		7000-0221	WASHER			#4	
25					1		0285-0195-20	WIRE ASSY				LM
26					1		0285-0196-20	WIRE ASSY				LM
27					1		6600-0129	SWITCH	S3			
28					1		0114-0321	LABEL				
29					1		0285-0010-20	PW ASSY				LM
30					2		1300-0054	TRANSISTOR	Q7,8		2N6545	
31					1		0285-0010-20	PWB ASSY				LM
32												
33												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
G	REVISED PER ECO # 1781	8/24	MZ		
H	REVISED PER ECO # 1665	8/24	MZ		
J	REVISED PER ECO # 1859	8/28	MZ		
K	REVISED PER ECO # 1853	8/24	MZ		
L	REVISED PER ECO # 2001	8/24	MZ		
M	REVISED PER ECO # 2018	11-1781	MZ		
N	REVISED PER ECO # 2152	11-1781	MZ		

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

	DATE
DRAWN E. SANDELL	2-81
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
POWER SUPPLY
TOP ASSEMBLY

biomation

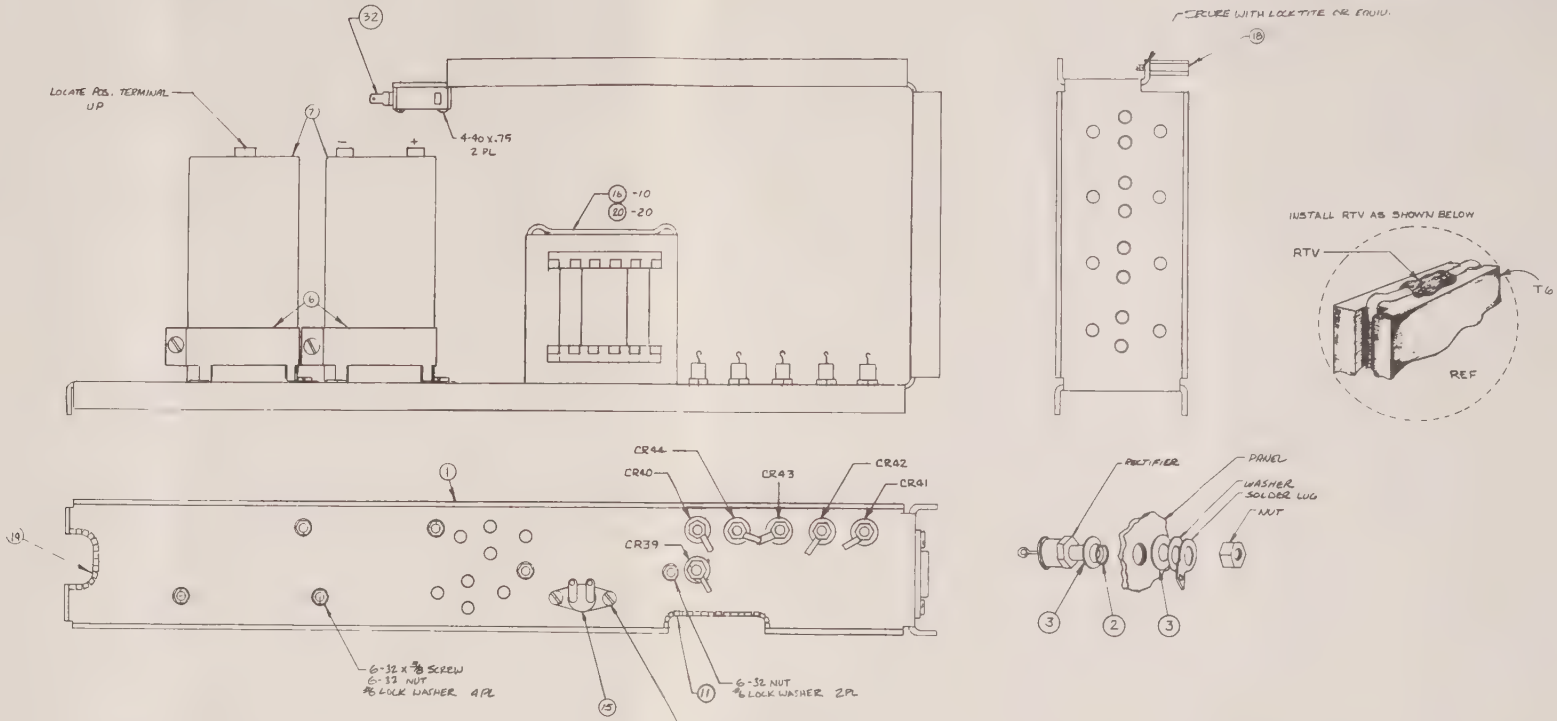
B | 0285-0003 | REV T

MODEL 4500 | CODE | SHEET 2 OF 2

DWG. NO. 0285-0173 | SH 1 | REV Q

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	Q	3600A	REVISED PER ECO	MW	DLW	[illegible]
	B	1472	REVISED PER ECO	MB	RD	9-29-81
	C	1476	CANCELLED (NO CHANGE TO ASSY)	PRS	—	—
	D	1547	REVISED PER ECO.	MB	RD	9-6-81
	E	1567	REVISED PER ECO.	MB	RD	5-8-81
	F	1696	REVISED PER ECO	JWC	RD	4-30-81
	F	ERN 0152	PRODUCTION RELEASE	JWC	RG	7-28-81
	G	1784	NO CHANGE. (ECO ERROR)	MB		7/6/81
	H	1785	REVISED PER ECO	MB	[illegible]	6-11-81
	J	1834	REVISED PER ECO.	MB	[illegible]	6-15-81
	K	1665	REVISED PER ECO	[illegible]	RD	
	L	2418	REVISED PER ECO	[illegible]	RD	
	M	2484	REVISED PER ECO No	[illegible]	[illegible]	4-14-82
	N	2733	REVISED PER ECO NO	[illegible]	DLW	
	P	3583	REVISED PER ECO No	JWC	DLW	3-15-83



NOTES: UNLESS OTHERWISE SPECIFIED:

1. MYLAR TAPE, ITEM 21, TO BE PLACED ON CAPACITORS, ITEM 7, BEFORE BRACKETS, ITEM 6.

DASH NO	NUMBER	QTY
-20	0285-0103-20	1
-10	" " -10	1

NEXT ASSEMBLY

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER VOIDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES; .XX ± .020 ± 1°; .XXX ± .010

HOLE SIZE: 1 .500 ± .003; .005 .000 ± .004; 1 .000-1 .000 ± .001

ENG. SERV. [illegible] DATE 5/29/81

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DRAWN SANDELL DATE 11 20 80

CHECKED [illegible] 5/29/81

PROJ. ENG. [illegible] 6/5/81

MANUFACTURING [illegible] 6/3/81

QUALITY ASSUR [illegible] 6/3/81

GOULD biomation

TITLE ASSY, HEATSINK

SCALE FULL | SIZE D | PART NUMBER 0285-0173 | REV Q

CODE 4500 | SHEET 1 OF 1

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1					1		0285-0176	HEAT SINK				
2					6		7000-0441	BUSHING	CR39-43			
3					12		7000-0442	WASHER	CR39-43		MICA	
4												
5												
6					2		7000-0464	BRACKET				
7					2		4400-0046	CAP	C12, 13		2000MF 200V	
8					2		1200-0015	RECTIFIER	CR43, 44	IN5826		
9					4		1200-0036	RECTIFIER	CR39, 40, 41, 42	IN6095		
10												
11					A/R		7200-0044	FLEX GROMET		SP42-2		
12												
13												
14					1		6600-0121	SWITCH	S2			
15					1		6600-0014	ELKWOOD SENSOR				
16												LM
17												
18					3		7000-0421	STAND-OFF			MALE/FEMALE	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL PER ERN #0082		JKP		
P	REVISED PER ECO No 3583	3/5/83	MW	DW	
Q	REVISED PER ECO No 3600A	3/9/83	MW	DW	3/9/83
D	REVISED PER ECO 1547	3-26-81	MK	RD	
E	REVISED PER ECO 1567	3-26-81	MK	RD	
F	REVISED PER ECO # 1696	4-30-81	MK	RD	
F	PROD REL. PER ERN No 0152	5-28-81	MK	RG	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-20	0285-0003-20	1
-10	0285-0003-10	1

	DRAWN	DATE
	J. PERGINS	3/9/81
	CHECKED RG	3/9/81
	ENGINEER	6/5/81
	MANUFACTURING	6/3/81
	QUALITY ASSURANCE	6/3/81

LIST OF MATERIAL

HEAT SINK ASSY

biomation

B | 0285-0173 | REV Q

MODEL 4500 | CODE | SHEET 1 OF 2

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19												
20					1		9000-0100-20	TRANSFORMER ASSY				LM
21												
22												
23												
24												
25												
26												
27												
28												
29												
30												
31												
32												
33												
34												
35												
36												

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
G	ECO 1784 NO CHANGE (ECO ERROR)	11-4-81	MS		
H	REVISED PER ECO #1785	7-13-81	MK	DW	7/13/81
J	REVISED PER ECO #1834	8-13-81	MK	DW	8/13/81
K	REVISED PER ECO # 1665	9-22-81	MK	RD	
L	REVISED PER ECO # 2418	9-24-82	MK	RD	
M	REVISED PER ECO No 2432	11-16-82	MK	DW	
N	REVISED PER ECO 2733	11-17-82	MK	DW	

DASH NO	NUMBER NEXT ASSEMBLY	QTY

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL

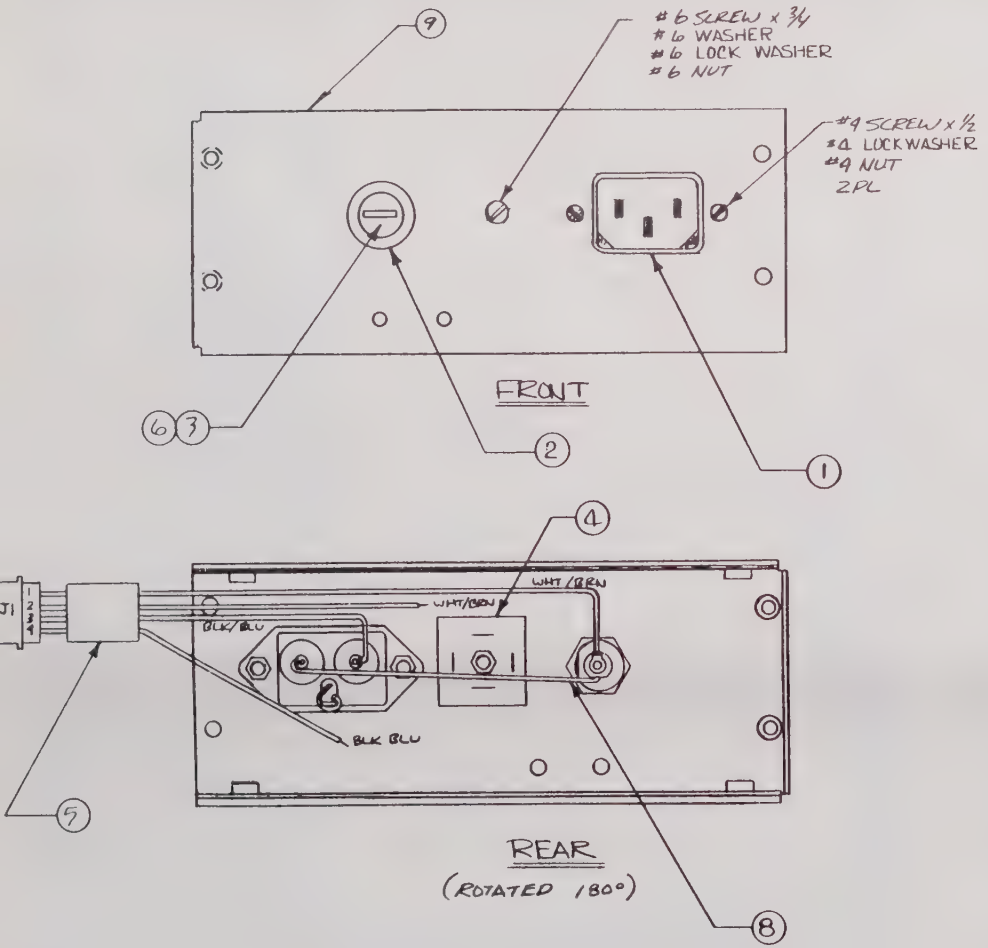
HEATSINK ASSY

biomation

B | 0285-0173 | REV G

MODEL 4500 | CODE | SHEET 2 OF 2

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL PER ERN № 0082	SWC	RD	11-18-80
	B	1522	REVISED PER ECO.	MB	RD	3-11-81
	B		PROD REL PER ERN № 0128	SR	RG	4-10-81
	C	1670	REVISED PER ECO	SWC	JL	4-20-81



ITEM	DESCRIPTION/SPECIFICATION	PART NAME	PART NUMBER
1			

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES; XX ± .020 ± 1°; XXX ± .010
HOLE SIZE: 0 599 + .003; 600 999 + .004; 1.000 1.499 + .005

DASH NO.	NUMBER	QTY
-10	0285-0003-20	1
-10	0285-0008-10	1
	NEXT ASSEMBLY	

		DATE
DRAWN	J WCARROLL	11-18-80
CHECKED	R Ligon	4/15/81
PROJ. ENG		4-15-81
MANUFACTURING	S Charlton	4-10-81
QUALITY ASSUR		4-10-81
ENG. SERV.	R. Ligon	9/10/81

GOULD biomation

TITLE: ASSEMBLY FACE PLATE

SCALE	SIZE	PART NUMBER	REV
NONE	C	0285-0156	C

CODE 28501 SHEET 1 OF 1

DWG NO 0285-0156 REV C

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	6000-0047	POWER CONN				
2						1	7300-0018	FUSE HOLDER SOCKET				
3						1	7300-0019	CARRIER				
4						1	1200-0034	BRIDGE	CR 35		400 V, 30A	
5						1	0285-0192	WIRE ASSY				LM
6						1	7300-0028	FUSE			6AMP 3 AG	
7												
8						1	0285-0193	WIRE FAB				
9						1	0285-0172	FACE PLATE				
10												
11												
12												
13												
14												
15												
16												
17												
18												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT PROD REL PER ERN 0082		DRS	RD	
B	REVISED PER ECO 1822	12-10-81	MB	RG	
B	PROD REL PER ERN #0128	4-10-81	SR	RG	
C	REVISED PER ECO # 1670	6-2081	JWC	JL	

DASH NO	NUMBER	QTY
-10	0285-0003-10	1
-10	0285-0003-20	1
NEXT ASSEMBLY		

DRAWN J.W. CARROLL 11-18-80
CHECKED R. Dean 4/15/81
ENGINEER D. Scott
MANUFACTURING S. Chapman 4-10-81
QUALITY ASSURANCE C. Lotz 4-10-81
R. Dean 4/10/81

LIST OF MATERIAL
ASSEMBLY
FACE PLATE

biomation

B | 0285-0156 | REV: C

MODEL 2850 5101 5200 | CODE | SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0287-0182	P.C.B			2850 FILTER BD	FAB
2						9	9000-0074	INDUCTOR	L2-6			LM
3						7	4000-0025	CAP	C1-7		.1uf CERAMIC	
4						1	6000-0410-20	CONNECTOR	J1		20 PIN RT ANG HDR N/L	
5						4	6400-0039	LED	DS 6-9		RED	
6						5	6400-0046	LED	DS 1-5		GRN	
7						1	3000-1006	RESISTOR	R7		10Ω 1/4W 5%	
8												
9												
10						2	3000-2701	RESISTOR	R1,2		2.7K 1/4W 5%	
11						1	3000-3906	" "	R3		39Ω "	
12						2	3000-1500	" "	R4,9		150Ω "	
13						1	3000-1801	" "	R6		1.8K "	
14						2	1200-0017	RECTIFIER	CR1,2		MR 751	
15												
16												
17												
18												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
B	REVISED PER ECO No 2736	1-7-83	JWC		
A	REVISED PER ECO 3585A	5-11-82	MW	RG	6-17-82
-	REVISED PER ECO NO 1738	7-20-81	JWC	RG	
C	PROD REL PER ERN #0192	6-2-81	JWC	RG	
D	REVISED PER ECO # 1946	8-24-81	JWC	RG	9-10-81
E	REVISED PER ECO # 2089	10-7-81	TMB	TMB	
F	REVISED PER ECO # 2419	4-1-82	JWC	RD	

DASH NO	NUMBER	QTY
-10	0285-0003-20	1
NEXT ASSEMBLY		

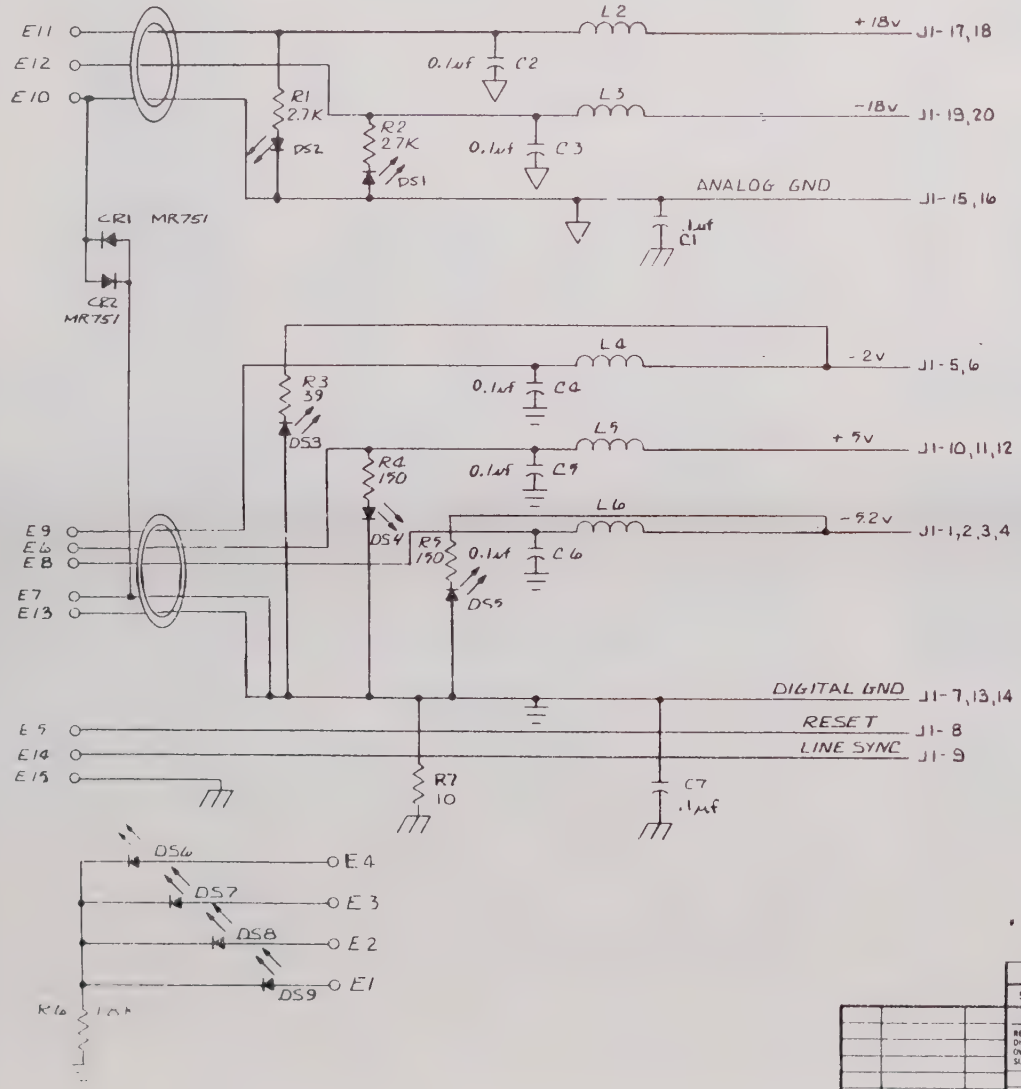
DRAWN J.W. CARROLL 5-28-81
CHECKED R.G. 6/2/81
ENGINEER
MANUFACTURING D. Scott 6/3/81
QUALITY ASSURANCE 6/3/81

LIST OF MATERIAL
FILTER BRD

biomation

B | 0285-0180 | REV: H

MODEL 4900 | CODE | SHEET 1 OF 1



REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PROTO TYPE	JWC		11-18-80
	B		ADDED CR1,2, DELETE URB PILOT REL PER ERN 0122	DRS	JL	12-2-81
	C	1738	REVISED PER ECO Nº	JWC	RG	6-2-81
	C	—	PROD REL PER ERN 40152	JWC	RG	6-2-81
	D	1901	REVISED PER ECO	SR	RD	8-13-81
	E	2089	REVISED PER ECO	KL	[illegible]	10-8-81
	F	2674	REVISED PER ECO N/O	JWC	[illegible]	12-1-82
	—	—	SKIPPED REV 'G'	MW		
	H	3585A	REVISED PER ECO	MW	[illegible]	6-17-83

NOTES:

UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITORS ARE IN MICRO FARRADS
3. ANALOG GROUND ▽
4. DIGITAL GROUND ⏚
5. ALL DIODES ARE:

DWG NO. 0285-0181 REV H

DASH NO	NUMBER	QTY
10	0285-0180	1
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: X ± 1, ANGLES; XX ± .020, 1°; XXX ± .010
HOLE SIZE: 0-.399 .003; .400-.999 .004; 1.000-1.499 .005

	NAME	DATE
DRAWN	SWCARROLL	11-18-80
CHECKED	RG	6/2/81
PROJ ENG	[illegible]	6/3/81
MANUFACTURING	[illegible]	6/8/81
QUALITY ASSUR	[illegible]	6/3/81
ENG SERV	RG	6/2/81

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

GOULD biomation

TITLE: POWER SUPPLY SCHEMATIC FILTER BD

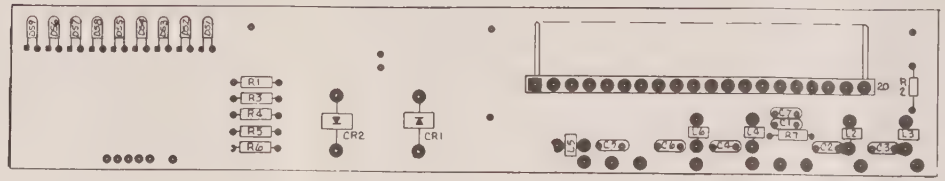
SCALE	SIZE	PART NUMBER	REV
NONE	C	0285-0181	H

CODE 4500 SHEET 1 OF 1

DWG. NO. 0285-0180 | SH. 1 | REV. H

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	B		PILOT REL PER ERN 0122		JL	
	C	1738	REVISED PER ECO Nº	JWC	RG	5-28-81
	C		PROD REL PER ERN 0172	JWC	RG	6-2-81
	D	1946	REVISED PER ECO #	[illegible]	MB	7-14-81
	E	2089	REVISED PER ECO	[illegible]	[illegible]	
	F	2419	REVISED PER ECO Nº	JWC	RD	4-1-82
	G	2736	REVISED PER ECO Nº	JWC	JW	1-7-83
	H	3585A	REVISED PER ECO	HW	[illegible]	6-17-83



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL ± ANGLES ±.5 ±.005 ±.1° ±.01 ±.010

HOLE SIZE 0.199 - .003 .000 .199 - .004 .000 .499 - .005

DASH NO	NUMBER	QTY
-10	0285-0063	1
	NEXT ASSEMBLY	

ENG SERV RG | DATE 6/2/82

DRAWN JWC SANDELL | DATE 6-2-81

CHECKED RG | 6/2/81

PROJ ENG. [illegible] | 6/5/81

MANUFACTURING [illegible] | 6/3/81

QUALITY ASSUR [illegible] | 6/3/81

GOULD biomation

TITLE ASSY POWER SUPPLY FILTER BD

SCALE 2/1 | SIZE D | PART NUMBER 0285-0180 | REV H

CODE 4700 | SHEET 1 OF 1

DWG. NO. 0285-0011 | SH 1 | REV KL

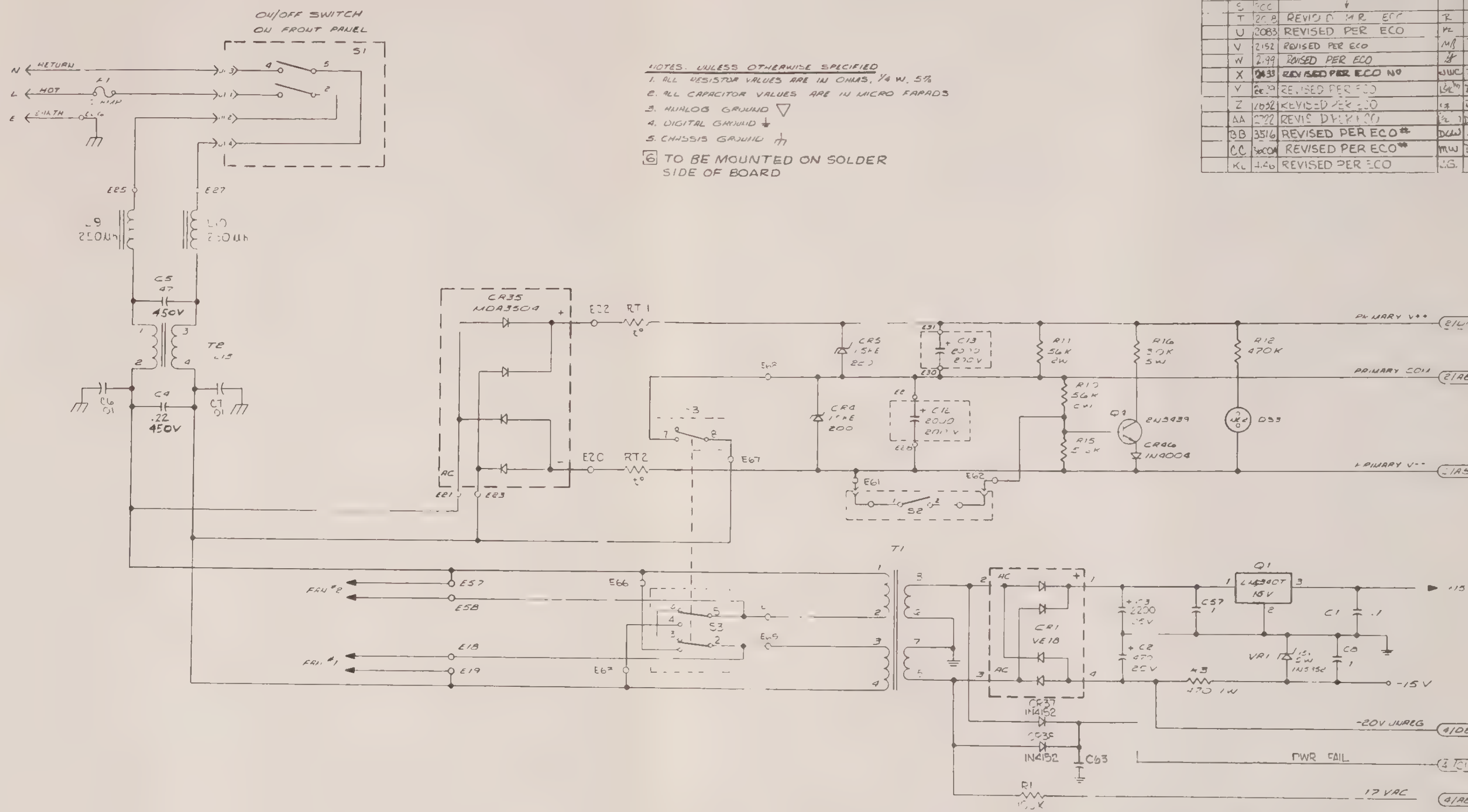
REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	M	1781	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	N	1785	" " "		[illegible]	
	P	[illegible]			[illegible]	
	Q	[illegible]			[illegible]	
	R	[illegible]			[illegible]	
	S	[illegible]			[illegible]	
	T	[illegible]	REVISED PER ECO	R	[illegible]	[illegible]
	U	2083	REVISED PER ECO	[illegible]	RD	[illegible]
	V	2152	REVISED PER ECO	MB	RD	[illegible]
	W	2199	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	X	2433	REVISED PER ECO NO	JWC	T.T.	[illegible]/82
	Y	[illegible]	REVISED PER ECO	[illegible]	DLW	
	Z	[illegible]	REVISED PER ECO	[illegible]	DLW	
	AA	[illegible]	REVISED PER ECO	[illegible]	DLW	
	BB	3516	REVISED PER ECO#	DLW	—	—
	CC	[illegible]	REVISED PER ECO#	MW	DLW	[illegible]
	KL	[illegible]	REVISED PER ECO	J.G.		

NOTES. UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS
3. ANALOG GROUND ▽
4. DIGITAL GROUND
5. CHASSIS GROUND

[6] TO BE MOUNTED ON SOLDER SIDE OF BOARD



				1
50 40 30 20 10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM

DO NOT SCALE DRAWING

TOLERANCE

DRAWN	DATE
J. PERGINS	6/4/81
CHECKED	
PROJ ENG.	
MANUFACTURING	
QUALITY ASSUR	

ENG SERV | DATE

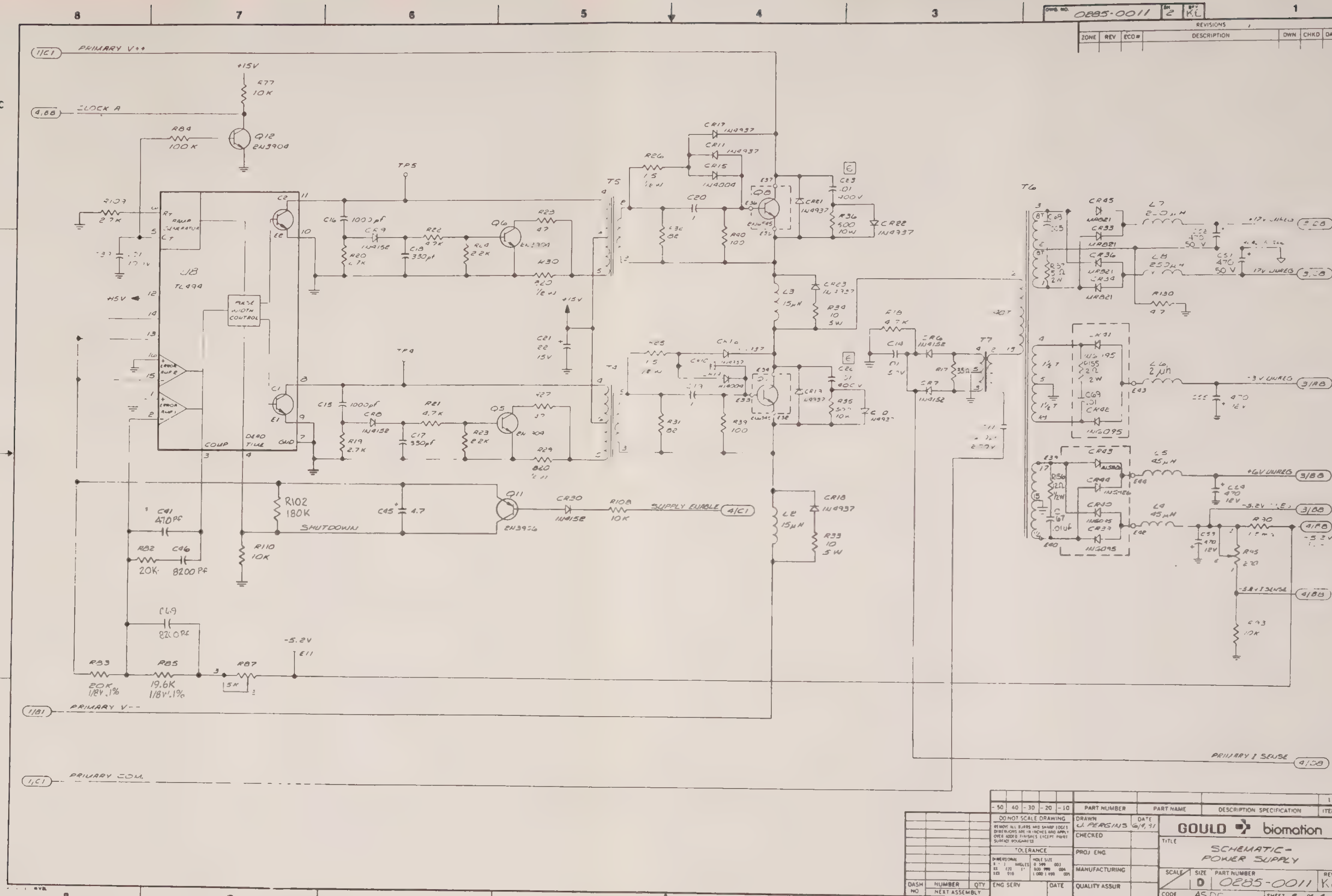
DASH NO | NUMBER | QTY — NEXT ASSEMBLY

GOULD biomation

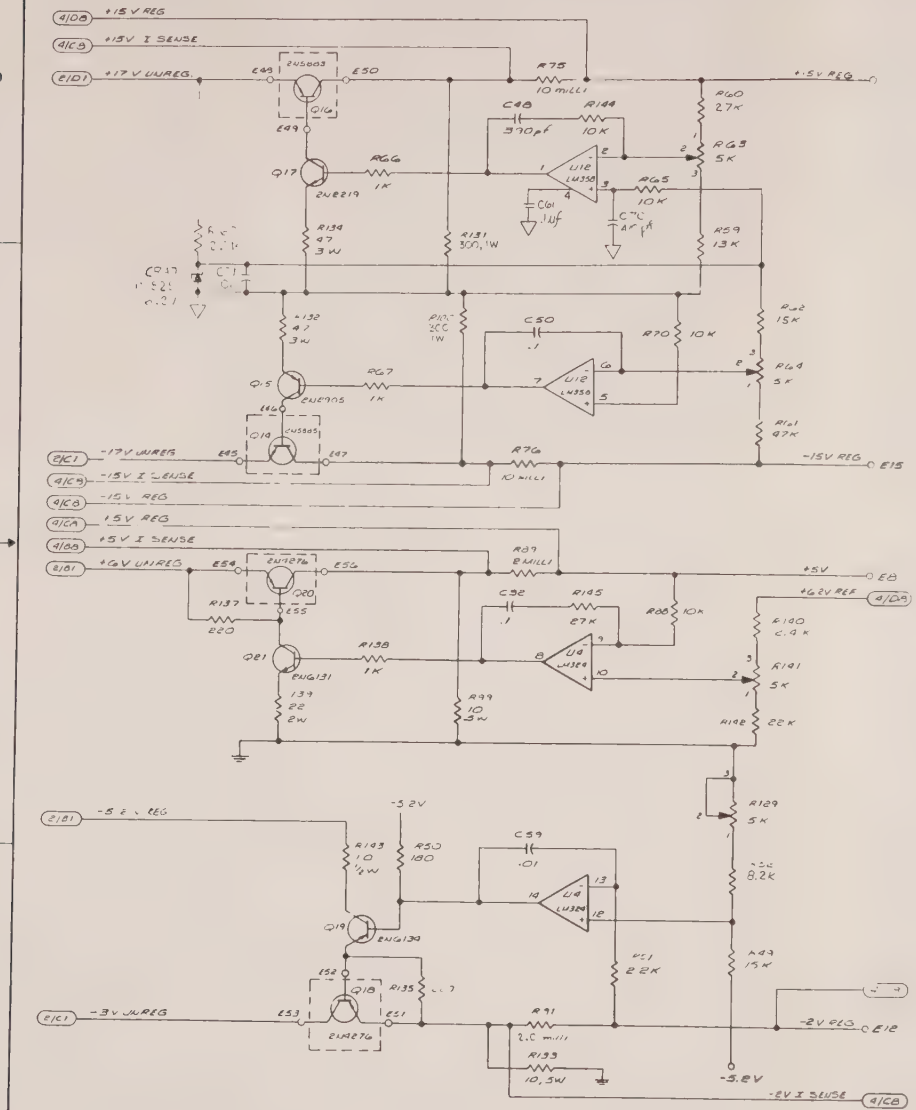
TITLE: SCHEMATIC - POWER SUPPLY

SCALE | SIZE D | PART NUMBER 0285-0011 | REV KL

CODE 4500 | SHEET 1 OF 4



0285-0011
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
PRIMARY V++
CLOCK A
+15V
R77 10K
R84 100K
Q12 2N3904
TP5
R107 2.7K
U8 TL494
RAMP GENERATOR
PULSE WIDTH CONTROL
ERROR AMP
COMP
DEAD TIME
GND
+5V
C16 1000pf
R22 4.7K
C19 330pf
R20 2.7K
Q6
R23 47
R30 820
T5
C20
R26
CR17 1N4937
CR11 1N4937
CR15 1N4004
Q8
CR21 1N4937
R36 500 10W
CR22 1N4937
C23 .01 400V
R40 100
L3 15µH
CR23
R34 10 5W
+15V
C21 22 15V
TP4
C15 1000pf
CR8 1N4152
R21 4.7K
C17 330pf
R19 2.7K
Q5
R29 820
R39 100
R31 82
R35
C26 .01 400V
R18 4.7K
C14
CR26 1N4152
CR27 1N4152
T7
T6
CR45
CR33
UR821
L7
CR36
CR34
L8
C51 470 50V
17V UNREG
R130 47
CR41
R155 2Ω 2W
C69 .01
CR42
1N5095
L6 2µH
-3V UNREG
CR43
CR44
L5 45µH
+6V UNREG
C54 470 12V
CR40
CR37
L4 45µH
-5.2V
C57 470 12V
R70
R45 270
-5.2V SENSE
R93 10K
R102 180K
C45 4.7
Q11 2N3906
CR30 1N4152
R108 10K
SUPPLY ENABLE
SHUTDOWN
C41 470PF
R82 20K
C46 8200PF
R110 10K
CR18 1N4937
L2 15µH
R33 10 5W
C49 8200PF
R83 20K 1/8W .1%
R85 19.6K 1/8W .1%
R87 5K
-5.2V
E11
PRIMARY V--
PRIMARY COM.
PRIMARY I SENSE
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION SPECIFICATION
ITEM
DRAWN
J. PERGINS
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
GOULD biomation
TITLE
SCHEMATIC-POWER SUPPLY
SCALE
SIZE D
PART NUMBER 0285-0011
REV
CODE 45OC
SHEET 2 OF 4
DASH NO
NUMBER
QTY
NEXT ASSEMBLY



DWG NO	SH	REV
0285-0011	3	KL

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM

DO NOT SCALE DRAWING

TOLERANCE

DRAWN	DATE
W. PERGINS	6/9/81
CHECKED	
PROJ ENG	
MANUFACTURING	
QUALITY ASSUR	
ENG SERV	DATE

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

GOULD biomation

TITLE: SCHEMATIC- POWER SUPPLY

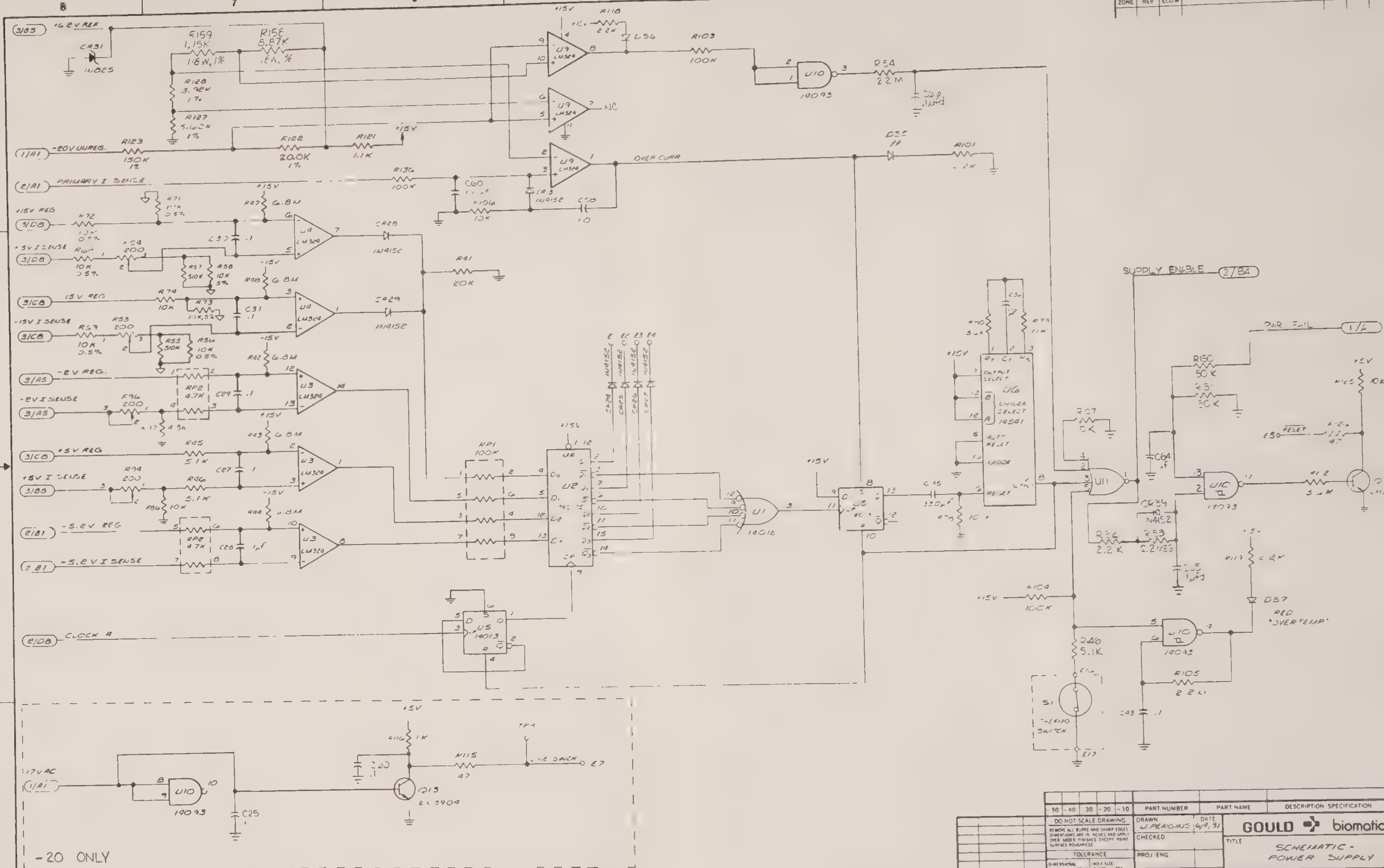
SCALE	SIZE	PART NUMBER	REV
	D	0285-0011	KL

CODE 45C60 SHEET 3 OF 4

0285-0011 | 4 | KL

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE



-50	-40	30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN J. PERKINS	DATE 6/4/81	
CHECKED		
PROJ ENG		
MANUFACTURING		
ENG SERV	DATE	QUALITY ASSUR

GOULD biomation

TITLE SCHEMATIC - POWER SUPPLY

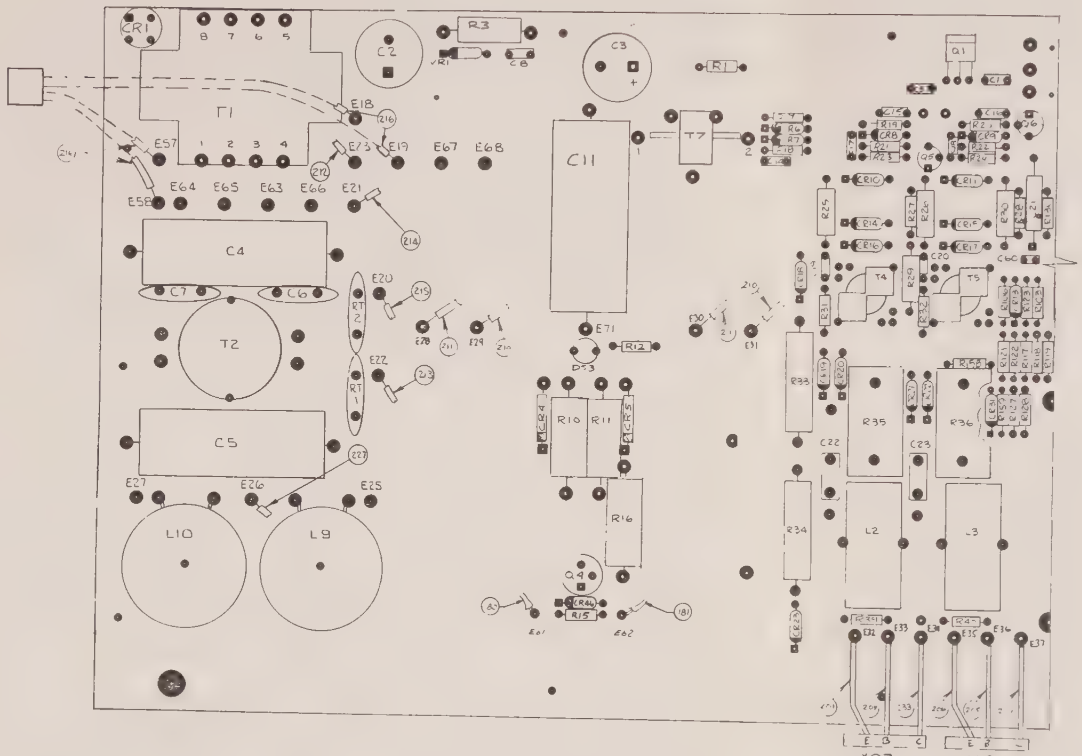
SCALE	SIZE	PART NUMBER	REV
	D	0285-0011	KL

CODE 4500 SHEET 4 OF 4

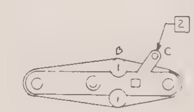
DWG NO 0285-0010 | SH 1 | REV KL

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	C		REDRAWN, PILOT REL PER ERN C-67	DRS	RD	3/4/81
	D	1486	CHANGES MADE PER ECO	TMB	RD	3/11/81
	E	1521	UPDATED PER PILOT RUN	TMB	RD	3/17/81
	F	1554	REVISED PER ECO	JO	RD	3-26-81
	G	1568	REVISED PER ECO	R.H.	RD	5-28-81
	H	1621	REVISED PER ECO	R.H.	RD	
	J	1636	REVISED PER ECO	R.H.	RD	
	K	1650	REVISED PER ECO	R.H.	RD	
	L	1629	REVISED PER ECO	R.H.	RD	
	M	1683	REVISED PER ECO	R.H.	RD	
	N	1697	REVISED PER ECO	R.H.	RD	
	P	1728	REVISED PER ECO	R.H.	RD	
	Q	1736	REVISED PER ECO	R H	RD	[illegible]
	Q	—	PROD REL PER ERN NO 152	[illegible]	RG	9-28-81
	R	1781	REVISED PER ECO	KL		
	S	1785	REVISED PER ECO	MS		[illegible]
	T	1831	REVISED PER ECO	KL		
	U	1853	REVISED PER ECO	KL		
	V	1859	REVISED PER ECO	KL		
	W	1980	REVISED PER ECO	KL		
	X	2018	REVISED PER ECO	KL		
	Y	2083	REVISED PER ECO	KL		
	Z	2152	REVISED PER ECO	MS		[illegible]
	AA	2199	REVISED PER ECO	[illegible]		
	BB	2420	REVISED PER ECO	[illegible]		
	CC	2433	REVISED PER ECO	[illegible]	T.J.	[illegible]/82
	DD	2508	REVISED PER ECO	[illegible]	T.J.	[illegible]/82
	EE	2629	REVISED PER ECO	[illegible]		
	FF	2632	REVISED PER ECO	[illegible]		
	GG	2722	REVISED PER ECO	[illegible]		
	HH	2733	REVISED PER ECO	[illegible]		
	JJ	3516	REVISED PER ECO *	DGW		
	KK	3600A	REVISED PER ECO *	[illegible]	DGW	[illegible]
	KL	4146	REVISED PER ECO	[illegible]		



LEFT SIDE



DETAIL A
REAR VIEW

NOTE

1. [illegible] ARE TO BE MOUNTED ON THE FAR SIDE OF THE [illegible]
2. DRILL OUT "C" HOLE (.125 DIA) ON XQ18 & XQ20.
3. SEE TOP ASSY 0285-0003.
4. (C22 & C23 TO BE MOUNTED ON THE SOLDER OF PCB)

PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DASH NO | NUMBER | QTY — NEXT ASSEMBLY

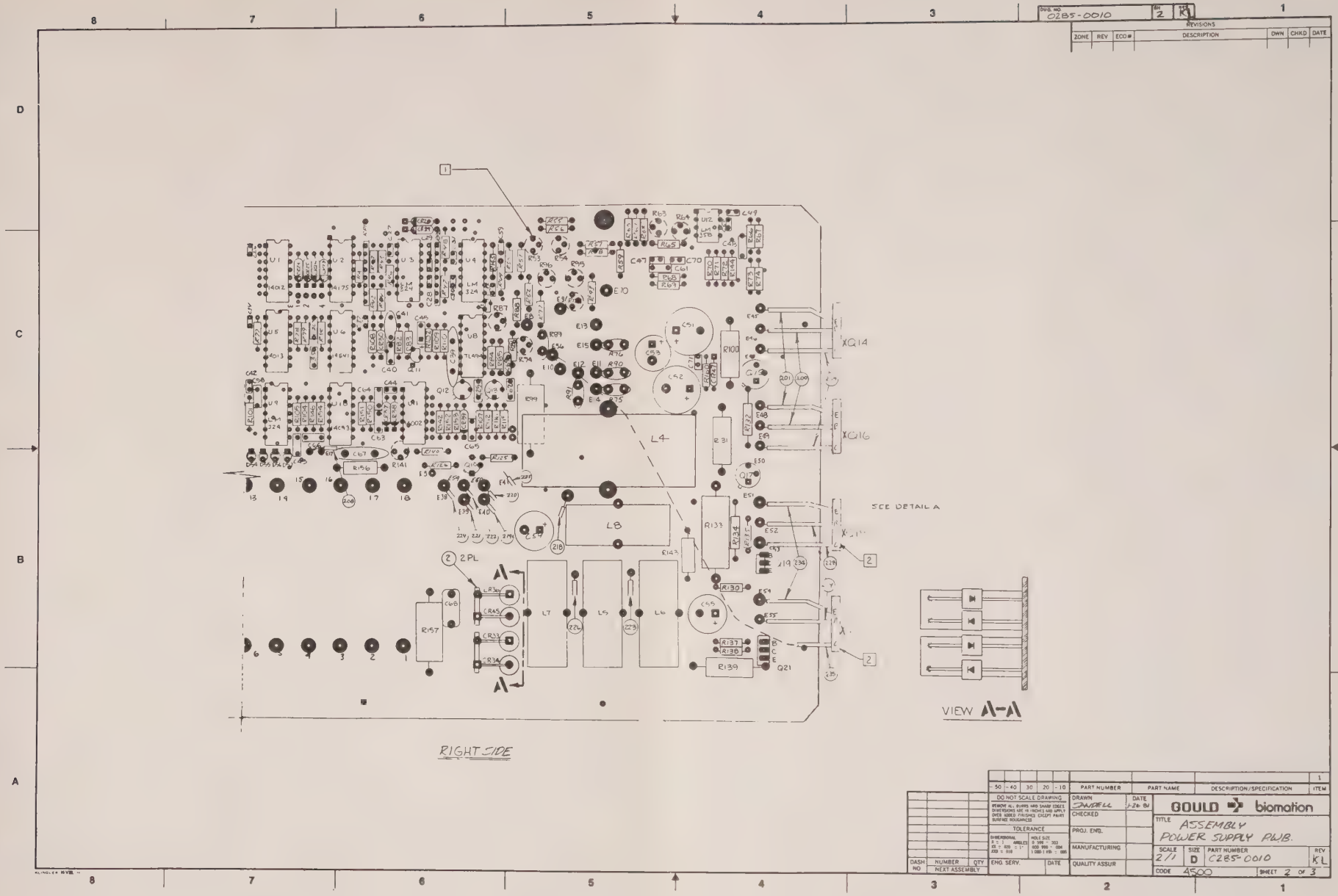
DRAWN		DATE
CHECKED	RG	5/29/81
PROJ. ENG.	[illegible]	6/5/81
MANUFACTURING	[illegible]	6/1/81
QUALITY ASSUR	[illegible]	
ENG SERV	RG	5/29/81

GOULD biomation

TITLE ASSEMBLY
[illegible] ER SUPPLY PWB

SCALE	SIZE	PART NUMBER	REV
1/1	D	0285-0010	KL

CODE 4500 — SHEET 1 OF 3


DWG. NO. 0285-0010
SH 2
REV KL
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
SEE DETAIL A
VIEW A-A
RIGHT SIDE
2 PL
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
DATE
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV.
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
ASSEMBLY
POWER SUPPLY PWB.
SCALE
2/1
SIZE
D
PART NUMBER
C285-0010
REV
KL
CODE
4500
SHEET 2 OF 3

WIRE LIST				
WIRE Nº	FROM	TO	ITEM Nº	DESCRIPTION
1				3
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16	E16		208	BRN
17	E17		208	RED
18	E18	P3	216	TAN
19	E19	P4	216	TAN
20	E20		215	BLK
21	E21		214	VIO
22	E22		213	YEL
23	E23		212	ORG
24	E24		N/C	—
25	E25		1	1
26	E26		227	GRN/YEL
27	E27		1	1
28	E28		211	RED
29	E29		210	BRN
30	E30		211	RED
31	E31		210	BRN
32	E32	XQ7 E	201	RED
33	E33	XQ7 B	204	BLK
34	E34	XQ7 C	202	BLK
35	E35	XQ8 E	206	RED
36	E36	XQ8 B	205	BRN
37	E37	XQ8 C	207	BLK
38				
39	E39		221	ORG
40	E59		222	ORG
41	E40		219	RED
42	E60		220	RED
43				
44	E42		219	BRN
45	E43		223	YEL
46	E44		226	WHT/RED
47	E45	XQ14 E	201	RED
48	E46	XQ14 B	200	BRN
49	E47	XQ14 C	204	BLK
50	E48	XQ16 E	201	RED
51	E49	XQ16 B	200	BRN
52	E50	XQ16 C	204	BLK
53	E51	XQ18 E	234	RED
54	E52	XQ18 B	204	BLK
55	E53	XQ18 C	233	BLK
56	E54	XQ20 E	236	RED
57	E55	XQ20 B	204	BLK
58	E56	XQ20 C	235	BLK
59	E57	P1	216	BLK
60	E58	P2	216	BLK
61	E61	—	180	BRN
62	E62	-	181	RED
63	E70	-	214	VIO
64	T6	E71	—	WHT (IF USED)

DWG. NO. 0285-0010 SH 3 REV KL

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PRINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES .XX ± .03 .XXX ± .010 HOLE SIZE: 0 .999 ± .003 .000 .999 ± .004 1.000 1.999 ± .005

DRAWN SANDFELL DATE 1-28-81

CHECKED

PROJ ENG

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE ASSY POWER SUPPLY P.W.B.

SCALE NONE SIZE D PART NUMBER 0285-0010 REV KL

CODE 4500 SHEET 3 OF 3

DASH NO | NUMBER | QTY | NEXT ASSEMBLY | ENG SERV | CATE

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1					1		0285-0012	PWB				~~FAB~~
2					2		0285-0376-01	HEAT SINK				
3					15		1000-0002	DIODE	CR6-9, 24-30, 13	37-39	IN4152	
4												
5					10		1200-0031	DIODE	CR10, 11, 16, 17,	19-23, 18	IN4937	
6												
7												
8					1		1200-0026	DIODE BRIDGE	CR1		VE18X	
9												
10					3		1200-0014	DIODE	CR14, 15, 46		IN4004	
11												
12					2		1100-0015	DIODE	CR 31, 47		IN825	
13					2		1100-0043	DIODE	CR4, 5		1.5KE220	
14												
15					1		1000-0022	DIODE	VR1		IN5352	
16					4		1200-0042-10	DIODE	CR33, 34, 36, 45		MR821	
17												
18												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE	11-16-83	MB	RG	
B	REDESIGNED			RD	
C	PILOT RUN PER ERN 0089			RD	
D	CHANGED PER ECO # 1486	3-10-84	TTM	RD	
E	UPDATED PER PILOT RUN ECO 1521	3-10-84	TTM	RD	
F	ECO 1534	3-27-84	MB	RD	
G	ECO 1568	4-20-84	TTM	RD	

DASH NO	NUMBER	QTY
-70	0285-0003	
	NEXT ASSEMBLY	

DRAWN M Burton 11-20-83
CHECKED R. Simpson 6/5/84
ENGINEER R.D. 6/5/84
MANUFACTURING J.K. Donald 6/3/84
QUALITY ASSURANCE [illegible] 6/3/84

LIST OF MATERIAL
POWER SUPPLY
ASSY - PWA

MODEL 4500

biomation

B | 0285-0010 | REV K L

CODE | SHEET 1 OF 13

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19												
20					A/R		8300-0002	MYLAR TAPE				
21					1		1300-0006	TRANSISTOR	Q17		2N2219	
22					5		1300-0028		Q5, 6, 10, 12, (Q13-20 ONLY)		2N3904	
23					1		1300-0035		Q21		2N6131	
24					1		1400-0003		Q15		2N2905	
25					1		1400-0026	TRANSISTOR	Q19		2N6134	
26												
27					1		1400-0019	TRANSISTOR	Q11		2N3906	
28												
29												
30												
31												
32					1		1300-0056	TRANSISTOR	Q4		2N3439	
33												
34					1		1700-0047	IC.	Q1		LM340T	
35					1		3700-0078	RES PACK	RP1		100K	
36					1		3700-0077	RES PACK	RP2		4.7K	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
J	ECO 1621	4-28-84	RH	RD	
K	ECO 1636	4-28-84	RH	RD	
L	ECO 1650	4-28-84	RH	RD	
M	ECO 1683	4-28-84	RH	RD	
N	ECO 1697	5-4-84	RH	RD	
P	ECO 1728	5-4-84	RH	RD	

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M Burton 11-20-83
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
POWER SUPPLY
ASSY PWA

MODEL 4500

biomation

B | 0285-0010 | REV K L

CODE | SHEET 2 OF 13

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
37												
38												
39												
40					1		1700-0096	I.C.	U12		LM358	
41					3		1700-0086	I.C.	U3,4,9		LM324	
42												
43					1		1820-0073	CMOS	U6		14541	
44					1		-0066		U2		14175	
45					1		-0002		U11		14002	
46					1		-0004		U1		14012	
47					1		-0017		U5		14013	
48					1		-0072		U10		14093	
49												
50												
51					1		1700-0095	I.C	U8		TL494	
52												
53					2		3600-0001-10	THERMISTOR	RT1, RT2		RL6606-3.28-52-52	
54												

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
Q	ECO 1736	5-14-81	[illegible]	RD	
Q	PRODUCTION REL PER ERN #0152	5-28-81	[illegible]	RG	
R	REVISED PER ECO #1781	8-24-81	MR	[illegible]	
S	REVISED; ECO #1785	6-10-81	MR	[illegible]	
T	REVISED; ECO #1831	8-24-81	MR	[illegible]	
U	REVISED; ECO #1853	8-24-81	MR	[illegible]	
V	REVISED; ECO #1859	8-24-81	MR	[illegible]	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M Burton — DATE 11-20-80
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
POWER SUPPLY
ASSY PWA

biomation

B 0285-0010 REV KL

MODEL 4500 — CODE — SHEET 3 OF 13

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
55												
56					2		3000-1503	RESISTOR	R150, 151		150K 1/4W 5%	
57					2		3000-1000	RESISTOR	R39, 40,		100Ω 1/4W 5%	
58					12		-1002		R65, 70, 77, 86, 88,		10K	
59									93, 106-108, 110, 125, 144			
60					6		-1003		R1, 78, 84, 103, 104, 136		100K	
61					1		-2202		R142		22K	
62												
63					3		-2204		R105, 154, 153		2.2MEG	
64												
65					1		-4301		R97		4.3K	
66					8		-2201		R23, 24, 51, 101, 117-119, 152		2.2K	
67					2		-2200		R135, 137		220Ω	
68												
69					1		-1800		R50		180Ω	
70					1		-1803		R102		180K	
71												
72					1		3000-1101	RES	R121		1.1K, 1/4W, 5%	

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
W	REVISED; ECO #1980	8-24-81	[illegible]	[illegible]	
X	REVISED PER ECO #2018	9/25/81	[illegible]	[illegible]	
Y	REVISED PER ECO #2083	10/25/81	[illegible]	[illegible]	
Z	REVISED PER ECO #2152	11/25/81	MR	[illegible]	
AA	REVISED PER ECO #2199	3-30-81	[illegible]	KL	
BB	REVISED PER ECO #242	3-2-82	[illegible]	KL	
CC	REVISED PER ECO #2433	7/1/82	[illegible]	[illegible]	

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M Burton — DATE 11-20-80
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
POWER SUPPLY
ASSY PWA

biomation

B 0285-0010 REV KL

MODEL 4500 — CODE — SHEET 4 OF 3

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
73					1		3100-1962	RESISTOR	R85		19.6K, 1/8W, 1%	
74					1		3000-4703	RESISTOR	R12		470K 1/4W 5%	
75												
76					5		-6804		R42-44, 47, 48		6.8MEG	
77					2		3000-5103		R55, 57		510K,	
78					1		3000-2401	RES	R140		2.4K, 1/4W, 5%	
79					1		3000-2702	RES	R145		27K, 1/4W, 5%	
80												
81					4		-4706		R27, 28, 126 (R115-20 ONLY)		47Ω	
82												
83					3		-4701		R18, 21, 22,		4.7K	
84					3		-5601		R15, 80, 112		5.6K	
85					3		-5101		R45, 96, 146		5.1K	
86					4		3000-2701	RESISTOR	R19, 20, 109, 160		2.7K 1/4W 5%	
87												
88					2		3000-8206	RESISTOR	R31, 32		82Ω 1/4W 5%	
89												
90					1		3000-3306	RESISTOR	R17		33Ω 1/4W 5%	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	DD	REVISED PER ECO# 2508	9/14/79	JWL	T.J.	
	EE	REVISED PER ECO# 2629	11-17-81	CAP	DLW	
	FF	REVISED PER ECO# 2632	11 17 81	CAP	DLW	
	GG	REVISED PER ECO# 2722	11 17 81	CAP	DLW	
	HH	REVISED PER ECO# 2723	11 17 81	CAP	DLW	
	JJ	REVISED PER ECO# 3516	2-22-84	DLW	—	—
	KK	REVISED PER ECO# 3600A	3-9-84	MW	DLW	3/15/84

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL
POWER SUPPLY
ASSY PWA

MODEL 4500

biomation

B 0285-0010 REV K L

CODE

SHEET 5 OF 13

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
91												
92					1		3000-4702	RESISTOR	R61		47K 1/4W 5%	
93					1		-4707		R130		4.7Ω	
94					4		-1001		R66, 67, 138 (R116-20 ONLY)		1K	
95					2		-1302		R59, 62		13K	
96					1		-3302		R60		33K	
97					1		-1102		R79		11K	
98					2		3000-2002		R41, 82		20K 1/4W 5%	
99					2		3100-2002		R83, 122		20K 1/8W, 1%	
100					1		3000-8201	RESISTOR	R52		8.2K 1/4W 5%	
101												
102					1		3000-1502	RESISTOR	R49		15K 1/4W 5%	
103												
104												
105					1		3100-1503		R123		150K 1/8W, 1%	
106					1		3100 5621		R127		5.62K	
107					1		3100-3921	RESISTOR	R128		3.92K 1/8W 1%	
108												

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	KL	REVISED PER ECO 4146	12/[illegible]	J.G.		

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL
POWER SUPPLY
ASSY PWA

MODEL 4500

biomation

B 0285-0010 REV K L

CODE

SHEET 6 OF 13

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
110												
111					8		3120-1002	RESISTOR	R56,58,68,69,73,74		10K 1/8W .5%	
112									71,72			
113					1		3100-8871	RESISTOR	R158		8.87K,1/8W,1%	
114					1		3100-1151	RESISTOR	R159		1.15K,1/8W,1%	
115					2		3050-1507	RESISTOR	R25,26		1.5Ω 1/2W 5%	
116					2		-8200		R29,30		820Ω 1/2W 5%	
117												
118					1		3200-0039	RESISTOR	R139		22Ω, 2W	
119												
120					2		3070-3000	RESISTOR	R100,131		300Ω 1W 5%	
121					1		3070-4700	RESISTOR	R3		470Ω 1W 5%	
122					1		3050-1007	RESISTOR	R143		1Ω, 1/2W, 5%	
123					1		0285-0200-20	RESISTOR	R90		1.2MILLI OHM	
124												
125					2		3080-5602	RESISTOR	R10,11		56K 2W 5%	
126					1		3080-5106	RESISTOR	R157		51Ω 2W 5%	
127					1		3050-1206	RESISTOR	R156		12Ω 1/2W 5%	

REF DRAWINGS	REV.	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	M.K. Bost	11-20-80
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

POWER SUPPLY ASSY PWA

biomation

B | 0285-0010 | REV K L

MODEL 4500 | CODE | SHEET 7 OF 17

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
128												
129					1		3200-0037	RESISTOR	R16		3.0K 5W	
130					3		3200-0033	RESISTOR	R33,34,133		10Ω 5W	
131					2		3200-0035	RESISTOR	R35,36		500Ω 10W	
132					1		3080-3906	RESISTOR	R99		39Ω 2W 5%	
133												
134					2		0285-0199	RESISTOR COIL	R75,76		10 Milli Ohm	
135					2		0285-0200-10	RESISTOR COIL	R89,91		2 Milli Ohm	
136					2		3200-0038	RESISTOR	R132,134		47Ω 3W 5%	
137												
138					5		3300-0005	VAR. RESISTOR	R53,54,94-96		200Ω	
139					5		3300-0068	VAR. RESISTOR	R63,64,87,129,141		5K	
140												
141												
142												
143												
144												
145												

REF. DRAWINGS	REV.	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	M.K. Bost	11-20-80
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

POWER SUPPLY ASSY PWA

biomation

B | 0285-0010 | REV K L

MODEL 4500 | CODE | SHEET 8 OF 17

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
146												
147					1		4010-0101	CAPACITOR	C60		100 pf	
148					1		4010-0103	CAPACITOR	C14,		.01uf 50V	
149					3		4000-0049		C6, 7, 67		.01uf 1KV, 20%	
150					20		4000-0104		C1,8,19,20,27-32,43,		.1uf, 50V	
									50,57,61,63-66 (C25,62,-20 ONLY)			
152					10		4000-0044	CAPACITOR	R26,33,34,37,42,44,47,49,59,71		.01uf, 100V	
153					2		4200-0037	CAPACITOR	C22, 23		.01uf, 400V POLYPROPOLENE	
154					1		4200-0006	CAPACITOR	C39		.01uf, 100V	
155					1		4000-0007	CAPACITOR	C58		1uf, 50V	
156					3		4100-0015	CAPACITOR	C15, 16, 36		1000 pf, 500V	
157					3		4100-0018	CAPACITOR	C17, 18, 35		330 pf, 500V	
158					2		4010-0471	CAPACITOR	C70, 41		470pf 50V/100V	
159												
160					1		4300-0024	CAPACITOR	C45		4.7uf, 50V	
161					2		4010-0822	CAPACITOR	C40, 69		.0082uf, 50V, 10%	
162												
163												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M. Bo — DATE 11 20 80
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
POWER SUPPLY
ASSY PWA

biomation

B 0285-0010 REV KL

MODEL 4500 CODE SHEET 9 OF 13

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
164					1		4400-0037	CAPACITOR	C2		470uf 25V	
165					1		4100-0012	CAPACITOR	C48,		390 pf, 500V	
166					3		4400-0050	CAPACITOR	C53, 54, 55		470uf, 12V	
167					2		4400-0052		C51, 52		470uf/50V	
168					1		4300-0009		C21		22uf, 15V	
169												
170												
171					1		4200-0036		C11		6uf, 200V	
172					1		4000-0050	CAPACITOR	C68		.005 uf	
173					2		4200-0041	CAPACITOR	C4, 5		47uf, 400V	
174					1		4400-0051	CAPACITOR	C3		2200 uf, 25V	
175												
176												
177					4		6400-0039	L.E.D.	DS4, 5, 6, 7		RED	
178												
179												
180					1		0285-0221-10	WIRE ASSY				
181					1		0285-0221-20	WIRE ASSY				

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M. Bo — DATE 11 20 80
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
POWER SUPPLY
ASSY PWA

biomation

B 0285-0010 REV KL

MODEL 4500 CODE SHEET 10 OF 13

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
182					1		6400-0052	NEON LAMP	DS3	NE2		
183												
184												
185												
186					1		2500-0010-20	TRANSFORMER	T1		LINE XFMR 110/220 PRIMARY	
187					1		9000-0164	TRANSFORMER	T2,		INPUT BALUN XFMR 2213	
188					2		9000-0075	TRANSFORMER	T4, T5		BASE DRIVE XFMR	
189												
190					1		9000-0078	TRANSFORMER	T7		CURRENT SENSING XFMR	
191					1		9000-0079-20	INDUCTOR	L6		12μH	
192					2		9000-0077	INDUCTOR	L2, L3		SNUBBER INDUCTOR 2.4μH	
193					1		9000-0079-10	INDUCTOR	L5		HI-CURRENT OUTPUT INDUCTOR, 45μH	
194					2		9000-0080	INDUCTOR	L7, L8		LO-CURRENT OUTPUT INDUCTOR, 350μH	
195					1		9000-0083	INDUCTOR	L4			
196					2		9000-0165	INDUCTOR	L9, L10			
197												
198												
199												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN		11-20-80
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL
POWER SUPPLY
ASSY PWA

biomation

B | 0285-0010 | REV KL

MODEL 4500 | CODE | SHEET 11 OF 13

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
200					2		0285-0189-10	WIRE FAB			GRN	
201					3		-20				RED	
202					—		-30				BLK	
203					—		-40				RED	
204					5		-50				BLK	
205					1		-60				BRN	
206					1		-70				RED	
207					1		-80				BLK	
208					1		0285-0186	CABLE ASSY			RED BRN	LM
209												
210					2		0285-0185-10	"			BRN	LM
211					2		" -20	"			RED	LM
212					1		0285-0190-10	ASSY, Bridge WIRE			ORG	LM
213					1		-20	"			YEL	LM
214					1		-30	"			WHO	LM
215					1		-40	"			BLK	LM
216					1		0285-0191-10	CABLE ASSY, FAN			BLK, TAN	LM
217					—		0285-0189-91	CABLE FAB			BLK	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	SANCHEZ	12-2-80
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL
POWER SUPPLY
ASSY

biomation

B | 0285-0010 | REV KL

MODEL 4500 | CODE | SHEET/2 OF 13

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
218					1		0285-0201-01	RECT WIRE FAB			BRN	
219					1		-03				RED	
220					1		-04				RED	
221					1		-05				ORG	
222					1		-06				ORG	
223					1		-07				YEL	
224												
225												
226					1		-10				WHT/RED	
227					1		0285-0189-96	WIRE FAB			GRN/YEL	
228					—		0285-0189-92	WIRE FAB			BLK	
229					2		6100-0150	SOCKET	XQ18,20		.060 DIA. TERM.	
230					4		6100-0149	"	XQ7,8,14,16		.040 DIA TERM.	
231												
232					2		7200-0029	MOUSE TAIL			3" LONG	
233					1		0285-0334-10	CABLE ASSY			BLACK	
234					2		0285-0334-20	CABLE ASSY			RED	
235					1		0285-0334-30	CABLE ASSY			BLACK	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	SANDELL	DATE 1-27-81
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL
POWER SUPPLY
ASSY PWA

MODEL 4500

biomation

B | 0285-0010 | REV KL

CODE | SHEET 13 OF 13

MP MASTER
MA35373